TTM Operations and Technology Updates

Global Leader in PCB Manufacturing

TTM Technologies
Global Presence | Local Knowledge

Q2 -2013
Global Leader in PCB Manufacturing

Leading global PCB manufacturer - $1.3 billion in revenue*

15 specialized factories located in U.S. and China

Approximately 20,000 employees worldwide

Focused on advanced technology products

Total customer solution: prototype through production

Technology development coordinated with customers’ needs

Diversified end markets with broad customer base

¹ Based on 2012 sales
Specialized Facilities Provide Optimal Growth

Integrated manufacturing platform enables TTM to execute a global facility specialization strategy

**Aerospace/Defense**
1. Stafford, CT
2. Santa Clara, CA
3. San Diego, CA

**High Tech/Quick-Turn/High Mix**
4. Chippewa Falls, WI
5. Santa Ana, CA
6. Logan, UT
7. Hong Kong – OPCM

**Focused Assembly**
8. Shanghai, China
9. Stafford Springs, CT

**Volume Production**
10. Dongguan – DMC
11. Dongguan – SYE
12. Guangzhou – GME
13. Shanghai – SME
14. Suzhou – MAS

**Substrate**
15. Shanghai - SMST
PCB Manufacturing from A-Z

June 2013
IPC Designers Council RTP
PCB Manufacturing from A-Z Objective

- Provide an understanding of the processes involved in the manufacture of multi-layer printed circuit boards (PCB’s) from an independent viewpoint.
Early Supplier Involvement

- ESI
- DFV
- Pre-Prod. Eng.
- Inner Layers
- Lamination
- Hard Board
- Solder Mask & Legend
- Surface Finishes
- De-Panelize
- Inspection & Test
- New Technologies

Process Related
- Technology Roadmap Alignment
- Education and Training
- Specification Review

Part Related
- Technology Selection
- Panelization
- Impedance Stack-ups
- Design Rule Checks
Technology Selection (Part Number Specific)

- Working with suppliers to “get where you need to be” through
  - Impedance Stackup Modeling
  - Material Selection
  - Routing guidelines and Rules - DRCs
  - Interconnect Selection – Blind/Buried/Micro-vias
  - Part Size – Panelization

- Initiate Design Reviews, Kick Off Meeting and INVITE your suppliers to participate and offer suggestions BEFORE the design is finished.
Design for Value and Cost Avoidance

- ESI
- DFV
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- Inner Layers
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DFV Topics

- Aspect Ratio
- Layer Count
- Interconnects
- Material Selection
- Final Finish
- Panel Utilization
## Value Engineering Review – Part Number

<table>
<thead>
<tr>
<th>Material and Stackup Review</th>
<th>Y/N/ NA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Type</strong></td>
<td></td>
</tr>
<tr>
<td>Other material types available with similar electrical performance but with a lower cost?</td>
<td></td>
</tr>
<tr>
<td><strong>Copper foil Type</strong></td>
<td></td>
</tr>
<tr>
<td>Is there another copper foil type available with similar electrical performance but with a lower cost? (Like VLP -&gt; RTF)</td>
<td></td>
</tr>
<tr>
<td><strong>2 ply construction</strong></td>
<td></td>
</tr>
<tr>
<td>Could single ply construction be used in place of the 2 ply requirement?</td>
<td></td>
</tr>
<tr>
<td><strong>Resin Content</strong></td>
<td></td>
</tr>
<tr>
<td>Could a lower resin content be used?</td>
<td></td>
</tr>
<tr>
<td><strong>Impedance Traces</strong></td>
<td></td>
</tr>
<tr>
<td>Can any impedance requirements be consolidated? (Many trace requirements need many coupons to test and can reduce panel part real estate. By consolidating you could get extra units on the manufacturing panel.)</td>
<td></td>
</tr>
<tr>
<td><strong>Impedance Tolerances</strong></td>
<td></td>
</tr>
<tr>
<td>Is a an impedance tolerance specified that is tighter than standard industry practice? (i.e., +/- 10%)</td>
<td></td>
</tr>
<tr>
<td>Manufacturing Panel Review</td>
<td>Y/N/NA</td>
</tr>
<tr>
<td>-------------------------------------------------</td>
<td>--------</td>
</tr>
<tr>
<td>Panel Utilization</td>
<td>PCB units on the manufacturing panel. What is the panel size and the panel utilization? (over 65% is good)</td>
</tr>
<tr>
<td>Impedance Traces</td>
<td>Can any impedance requirements be consolidated? (Many trace requirements need many coupons to test and can reduce panel part real estate. By consolidating you could get extra units on the manufacturing panel.)</td>
</tr>
<tr>
<td>PCB Dimensions</td>
<td>Could small changes in the part size allow for another unit on the manuf panel?</td>
</tr>
<tr>
<td>Image Rotation</td>
<td>Does this part require image rotation? Did this impact the panel size selected?</td>
</tr>
</tbody>
</table>
## Value Engineering Review – Part Number

<table>
<thead>
<tr>
<th>PCB Design Parameter Review</th>
<th>Y/N/NA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer Reduction</td>
<td></td>
</tr>
<tr>
<td>Could the PCB have any layers reduced?</td>
<td></td>
</tr>
<tr>
<td>Surface Finish</td>
<td></td>
</tr>
<tr>
<td>Could another surface finish type be used to reduce costs?</td>
<td></td>
</tr>
<tr>
<td>Does this part require multiple surface finishes?</td>
<td></td>
</tr>
<tr>
<td>VIPPO</td>
<td></td>
</tr>
<tr>
<td>Does this part require VIPPO and is it actually required?</td>
<td></td>
</tr>
<tr>
<td>Backdrills</td>
<td></td>
</tr>
<tr>
<td>Does this part require multiple backdrill depths and can they be combined?</td>
<td></td>
</tr>
<tr>
<td>Does this part require backdrill from both sides of the PCB?</td>
<td></td>
</tr>
<tr>
<td>Can they be redone to only be from one side?</td>
<td></td>
</tr>
<tr>
<td>Sequential Lam</td>
<td></td>
</tr>
<tr>
<td>Doe the PCB require sequential lamination structures?</td>
<td></td>
</tr>
<tr>
<td>(Seq lam increases cost due to additional lamination, drill, and plating requirements)</td>
<td></td>
</tr>
<tr>
<td>Drill Size</td>
<td></td>
</tr>
<tr>
<td>Does the PCB Design specify drills that are not standard?</td>
<td></td>
</tr>
<tr>
<td>Or small drill bits that get rather expensive?</td>
<td></td>
</tr>
</tbody>
</table>
Manufacturing Panel Utilization

- Panel Utilization is one of the biggest opportunities for cost reduction.
- 5 - 40% reduction in board costs are possible.
- 70% and > utilization is considered good.

Buying the BOARDS.....

means paying for the Manufacturing PANEL
Pre-Production Engineering

- ESI
- DFV
- Pre-Production Engineering
- Inner Layers
- Lamination
- Hard Board
- Solder Mask & Legend
- Surface Finishes
- De-Panelize
- Inspection & Test
- New Technologies

Pre-Production Engineering Topics

- Data Package
- Data Receipt
- Planning
- CAM - DFM
- Waivers
Complete Data Package

- **Artwork Data:** ODB++ or RS274X (Gerber format with embedded aperture list).
- **Drill Data:** Excellon 1 & 2 (Separate drill file for each; PTH, NPTH, Blind.)
- **Board Outline:** RS274X or Excellon (milling file)
- **Array Layout Data:** RS274X or IPC-D-350
- **Fab Drawing:** HPGL or HPGL2 or RS274X
- **Aperture List:** Only needed with Gerber files (RS274)
- **Read-Me:** Company name, contact person(s), e-mail address, phone #, part number, file list, number format, units, layer name corresponding to file list
- **CAD Netlist:** IPC-D-356 or Vendor specific (Mentor Neutral File)
Data Receipt

- Data received in its raw form and read into the supplier’s CAM software tool
- Verify all the files needed exist and part numbers, etc. match
- Special apertures and drawn features are addressed
- Netlist comparison is completed as a Go/No Go
- Layers re-named for automated scripting to be successful
- Data is transferred to the CAM and Planning groups
Planning - Process Traveler

- Identifies the sequential steps required based on customer requirements
- Provides detailed information and specifications to the operators
- Traveler provides traceability throughout process
- Creates CAM instructions per customer specifications
  - Drill sizes
  - Scale Factors
  - Etch compensations

Part Number:xxx.xx
TTM #:xxxxx-xx-xx

- Step 1
- Step 2
- Step 3
- Step 4
- Step 5
Inner Layer Artwork Scaling

- Processing tends to “shrink” the material
- DOE results are used to calculate scale factors
- The factors are used for X & Y movement

"Stretched" X-Y location

Stretch factor

Desired location after lamination

Typical scale factors are from .0002” to .001” per inch (.0051mm to .0254mm per 25.4mm)
Etch Factors

Etched features are grown in order to compensate for loss during the etch process. (Factors differ from machine to machine & from vendor to vendor)

The following are approximate factors and do not account for special operations.

<table>
<thead>
<tr>
<th>Cu. Weight</th>
<th>Inner lyrs.</th>
<th>Outer lyrs.</th>
<th>Pattern Plate</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/2 oz.</td>
<td>.00025 (.006mm)</td>
<td>.0005 (.0127mm)</td>
<td></td>
</tr>
<tr>
<td>1 oz.</td>
<td>.00050 (.0127mm)</td>
<td>.001 (.0254mm)</td>
<td></td>
</tr>
</tbody>
</table>

Side-walls are unprotected from etchant and erode.
Fillets / Tear Dropping

- Tear dropping of via pads will increase circuit reliability
- Suggested size is 70% of pad with a .003 (.076mm) minimum extension
- If the pad to circuit junction requires greater A/R, add pad extensions
- Supplier CAM systems can add tear drops per your request
- Should be identified in specification for acceptability
Tool Creation

- Artwork (Film) Plotted
  - Finished board can only be as good as the artwork
  - Artwork size is affected by temperature and humidity

- Drill Program
  - Provides drilled hole location, size, feed & speed.
  - Drill “tool” for each “phase”; blind via, buried, PTH.

- Rout-Score Program
  - Rout or score files created from fab drawing or preferred milling file.

- Electrical Test Program and Fixture
  - Program created from netlist if provided or generated from Gerber design data
  - ET plates are drilled, pins “stuffed”
Supplier DFM - Waivers

- Comprehensive Design for Manufacturability analysis by supplier Pre-Production Engineering.

- “Show stopping” discrepancies, errors are documented and request to waiver submitted. Any waiver is a “Defect” of the Early Design Review process.

- 8 hour maximum turn around on deviation requested.
Top 10 Waiver Items 2012-2013 – TTM CF

1. Copper wrap plating below minimum design rule
2. Backdrill to copper below minimum
3. Drill tolerance for vias missing or very tight
4. Slot length tolerance below 5 mils
5. Thieving internal and external layers
6. Non Functional Pad removal
7. Allowance for tear dropping of vias
8. Backdrill stub length tolerance below minimum
9. Slivers on plane layers – cleanup below 3 mils
10. Print dimensions don’t match gerber or ODB ++ data

A typical design on average requires 3-4 waiver be addressed
Inner Layers

- ESI
- DFV
- Pre-Production Engineering
- Inner Layers
- Lamination
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Inner Layer Topics
- Material Release
- Resist Application
- Resist Exposure
- Resist Develop
- Copper Etching
- Resist Strip
- Post Etch Punch
- AOI
Material Release

- Appropriate material selected based on customer requirements – 370HR, Megtron 6, I-Speed, etc
- Material is chemically cleaned to remove protective coating.
Photo Resist Application

- Homogeneous thickness applied to both sides of panel.
- Can be either Liquid or “Dryfilm”.

Pressure and Heat Applied by Rollers

Exit Temperature

Core

Photo-resist is the medium used to transfer the image from the film to the actual PCB.
Resist Exposure

- Registration of the Photo-Tool (Artwork) to PCB - Glass/Mylar.
- Exposure of the photo-sensitive resist to H.I. Ultra-Violet Light 5-7Kw
- Polymerizes (hardens) the exposed areas of photo-resist.

Diagram:
- Polymerized Resist
- Tooled Glass
- Photo-Tool
- UV Light
- Core
Inner Layer Resist Exposure
Developing

- Conveyorized chemical spray system using mildly corrosive chemical to dissolve the un-polymerized photo-resist where copper foil is unwanted.
Copper Etching

Conveyorized chemical spray system using corrosive chemistry to etch away the unwanted copper. The photo resist protects the traces and pads from attack.
Strip Resist

- Conveyorized chemical spray system used to dissolve the polymerized photo-resist used to protect the copper during etching.
Post Etch Punch

- Optically registers to etched copper targets using an 8 camera system
- Compensates for movement incurred through etch
- Tooling holes punched after etch for best layer to layer registration
Automated Optical Inspection (AOI)

- Uses CAM data to verify printed board integrity.
- Marks defect location for review and possible repair.
Automated Optical Inspection - Detection Examples

- 7 mil mousebite, Bottom 6 to 7.1 mils actual
- 1 mil short, Top 0 to 4.1 mils actual 1.5 mils left in middle
- 3 mil pinhole, Top 1.7 mil inner actual 3.7 mil outer actual
- 3 mil open, Bottom 4.5 mils actual
Bonding the Layers - Lamination

- ESI
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**Lamination Topics**

- Oxide
- Lay Up
- Pressing - Lamination
- Tear Down
- Flash Rout
Oxide - Brown, Black, Alternative

Bare copper is chemically cleaned and treated to promote adhesion between the copper and the B-Stage during lamination.

“Brown” oxide process consists of cleaners, oxide, and typically a reducing agent to protect the oxide from acid attack (pink ring) during subsequent chemical processes such as electroless copper.

Oxide is conventionally performed using vertical “dip” tanks but in recent years alternative horizontal oxide systems have been developed that use micro-etching to promote adhesion to the b-stage.
Lay-Up

- Manual stacking of copper foil, b-stage, and core(s) between stainless steel or aluminum separator plates.
- Separators must be extremely flat and clean. Any debris will dent the PCB.
Vacuum Assist Hydraulic Lamination

Air is evacuated using a vacuum pump.

Multiple Boards in one Package

Separator Plate
Copper Foil

B-Stage
Copper Foil
Lamination Plate

Innerlayer
Innerlayer

Hot Press Platen - 350°F-300 PSI

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Lamination Press
Tear Down and Flash Rout

- The package of all panels or “book” is removed from the press and taken apart.
- The panels are inspected and measured for thickness.
- The resin that has been squeezed out of the package is called “flash” and must be cleanly routed off.
Hard Board - External Processing

- ESI
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- Pre-Production Engineering
- Inner Layers
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Hardboard Topics
- Drill
- Hole Prep
- Electroless Copper
- Resist Application
- Resist Exposure
- Resist Develop
- Pattern Plate Cu - Sn
- Strip - Etch - Strip
Drilling

- CNC mechanical drilling using designed drill data.
- Drilling Machines
  - Drilling equipment consists of 4 or 6 spindles each machine.
  - Pre-Production Engineering - Tools/Table Feed Rate/Bit RPM
  - The Table of the drill moves in X - Y, spindle only in Z - Axis
- Drill Bits
  - Smaller bits break easier and need changing more often.
  - Largest bit used in drilling is typically a .250” (6.35mm)
- X-Ray Machine used to verify hole to pad registration.
Drilling

- Aspect Ratio is **Board Thickness to Drill Size**

- Higher Aspect Ratio drive cost higher

\[ \frac{\text{Bd Thickness} = .093''}{.010'' \text{ Drill Size}} = 9.3:1 \text{ Aspect Ratio} \]

Entry Foil Reduces Burring

Drill Back-Up Material

Drill Table
Deburr - Desmear

- Hole and Surface Preparation for Electroless Copper.
- Deburr - Mechanical Abrasion /Cleaning of Copper Surface.
- Intense Water Pressure for Debris Removal from Hole.
- Removes Common Drill Burrs.
- Desmear - Chemical process of removing epoxy smear from the interconnects and micro-roughening hole wall.

Epoxy Smear

Dissolved for clean copper interconnect.

Copper

Dielectric
**Electroless Copper**

- Series of approx. 20 chemical & rinse tanks.
- Deposit palladium catalyst then electroless copper over all surfaces and in holes.
- Chemical reaction - no current - bussing
- High cost to operate.
- Environmental/Health & Safety concern.

“Backbone” of PCB.

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Dryfilm Lamination

- Process of applying a photo-sensitive film to both sides of the PCB. Photo-resist is generally .0025” thick

- Cut-sheet laminator puts a “postage stamp” on the panel, so plating border is open and tooling holes are not covered (automated).

Holes are covered over (tented) by resist during resist lamination
Dryfilm Exposure

- Registration of the Photo-Tool (Artwork) on glass to PCB
- Exposure of the photo-sensitive film to UltraViolet Light (5-7Kw)
- Polymerizes (hardens) the exposed areas of photo-resist.
Developing

- Conveyorized chemical spray system using mildly corrosive chemical to dissolve the un-polymerized photo-resist where copper plating is wanted.
Pattern Plating Copper

- Selectively plates copper using electrical current and an electrolyte. Sulfuric acid base, organic brightening and leveling System
- Current applied through buss bars connected to panel
  - Amperage per square foot (ASF) and time = Deposition
  - Part and solution agitation required for plating distribution

Copper plated in holes and on all exposed copper surfaces
Electrolytic Copper Pattern Plating

Buss Bar
Pattern Plating Tin

- Acid tin plating protects the copper pattern during etching

- Selectively plates tin using current and an electrolyte
  - Sulfuric acid base
  - Anodes - panel is cathode
  - Organic brightening and leveling system - distribution

- Current applied through buss bars connected to panel
  - Amperage per Square Foot (ASF) and time = deposition
  - Mechanical agitation improves plating distribution
Resist Stripping

Chemical spray system used to dissolve the polymerized photo-resist. This exposes the unwanted bare copper for etching.
Copper Etching

Removal of copper to form pattern using tin plating as etchant Resist

Spray Bar
Tin Stripping

Removal of the tin plating using corrosive acid to dissolve the tin.
Soldermask and Legend

- ESI
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Soldermask and Legend Topics

- Soldermask Application
- Soldermask Expose
- Soldermask Develop
- Legend Application
Soldermask Application

- The panel surface is cleaned to promote good adhesion.
- A homogeneous coating is applied to both sides.
  - Vertical double sided squeegee or
  - Spray method
Soldermask Exposure

- The phototool used to define pad openings is registered and vacuumed down in an exposure unit.
- The panel is then exposed to high intensity ultraviolet light.
Soldermask Develop

Conveyorized chemical spray system using mildly corrosive chemical to dissolve the un-polymerized solder-mask where final finish is desired - HASL/OSP, etc.
Legend – Nomenclature

- Liquid photoimagable ink (same process as soldermask)
- Traditional screen printing
  - The image is printed onto the screen.
  - The ink is squeegee through the screen openings onto the panel.
  - After the screening operation, the pattern is inspected and placed in an oven for thermal cure.
- Inkjet legend is also in wide use today – more economical and better image
Surface Finish Options

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Surface Finish Topics

- Selection Factors
- Finish Attributes
- Application Table
Final Finish Selection Factors

- Assembly process - soldering (wave/reflow), Au wire bond, etc.
- Pad surface flatness required - typically driven by pitch of component.
- Via Treatment – plugging impacts
- Cost effectiveness.
- Availability - supply base capability.
- Reliability data.
# Depanelize - Machining

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## Depanelize - Machining Topics

- Routing
- Scoring
CNC Routing

- Radius under .031” (.787mm) increase difficulty in manufacturing.
- Created from board outline file or fab drawing dimensions.
V-Scoring

- FR-4 <.045” (1.14mm) Approximately 30% of Material Remaining.
- Material Thickness Range = .010” - .125” (.254mm - 3.175mm)
Inspection & Test

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**Inspection & Test Topics**

- In Process Inspections
- Electrical Test
- Final Inspection
- Shipping
Product Inspection & Testing

- Line Width Measurements - Etching
- Automatic Optical inspection (AOI)
- X-ray - for Internal Registration after Drill
- X-ray of Plated or Deposited Metals for Comp. and Thickness
- TDR - Time Domain Reflectometry for Impedance Control
- Peel Strength for SM/Copper/Nickel & Gold Adhesion
- Micro-Sectioning for Thickness Measurements and PTH Quality
- Solderability and Thermal Shock
- Dimensional Measurements Bow & Twist, etc.
- Pin Gauges and CMI for Through Hole Size and Cu Thickness
- Ionic Contamination

There are hundreds and hundreds of process controls not mentioned due to time
Electrical Test Fixture (Bed of nails)
Electrical Test Fixture Assembly (Bed of nails)
Electrical Test
Final Inspection and Shipping - Documentation

- Visual Inspection and Dimensioning
- Proper packaging to assure product quality vacuum packaging to assure shelf life.
- Documentation included with package - test results, etc.
Thank You for your Time and Attention

- TTM has many tech bulletins/presentations covering more advanced topics:
  - Laminates and Foil from A-Z
  - Advanced Interconnect Selection (HDI)
  - Fabrication Topics for Si Engineers
  - Design for Value – Cost Avoidance
  - Flex and Rigid Flex Design
  - Many More

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