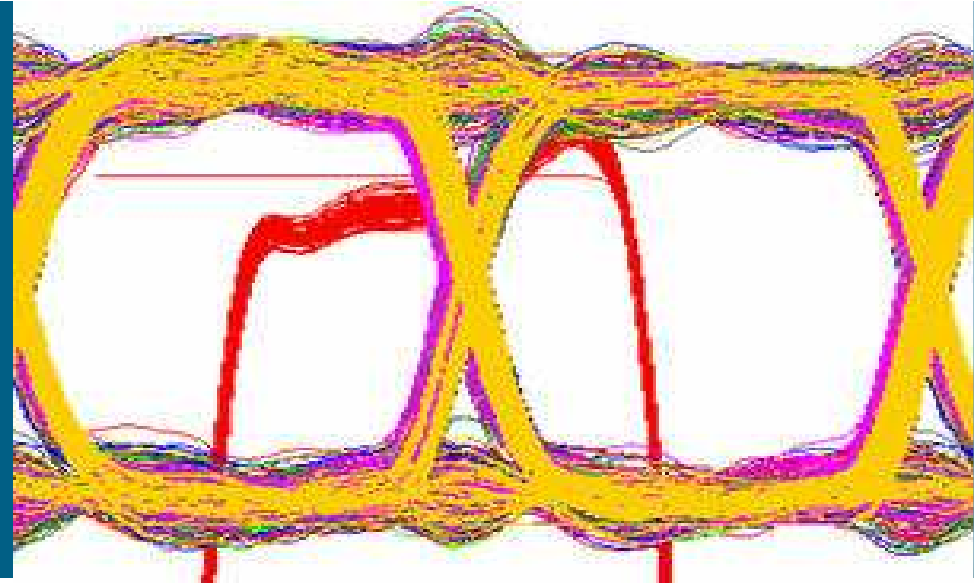




PCB level SI tools and strategy



Stephen Scarce
High Speed Design Team Manager
Cisco Systems Inc, RTP NC

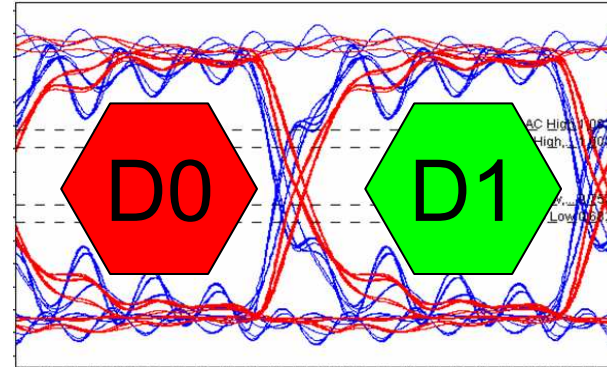
Q4 FY 2008

PCB level SI tools and strategy

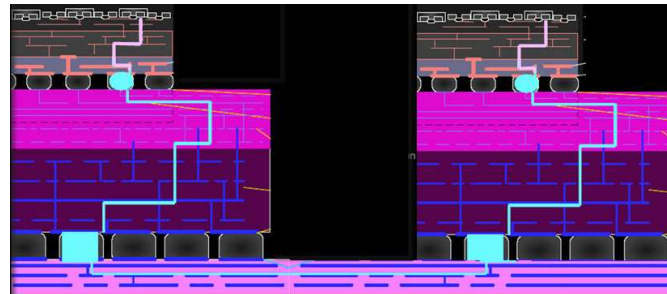
- Definition of HSD
- Static Timing Analysis for DDR
- Pre-route simulations (Scan the design space)
- Routing Rules development for CAD
- Full post route simulations
- Summary

What Is *High Speed Design*?

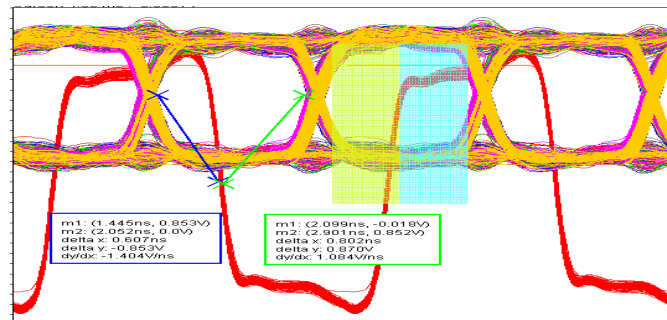
Getting the right data



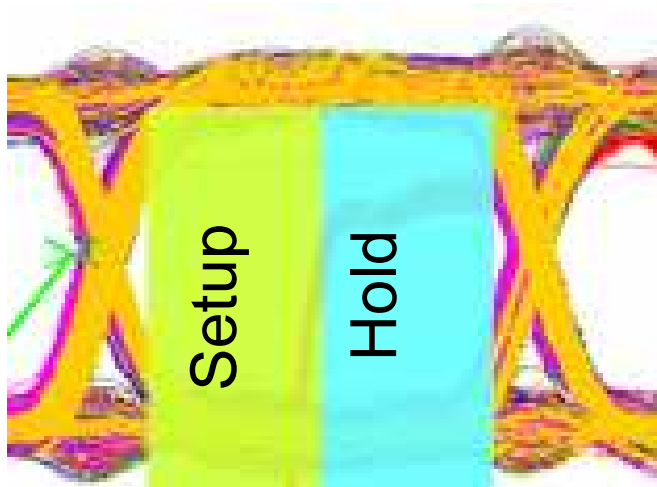
To the right place



At the right time



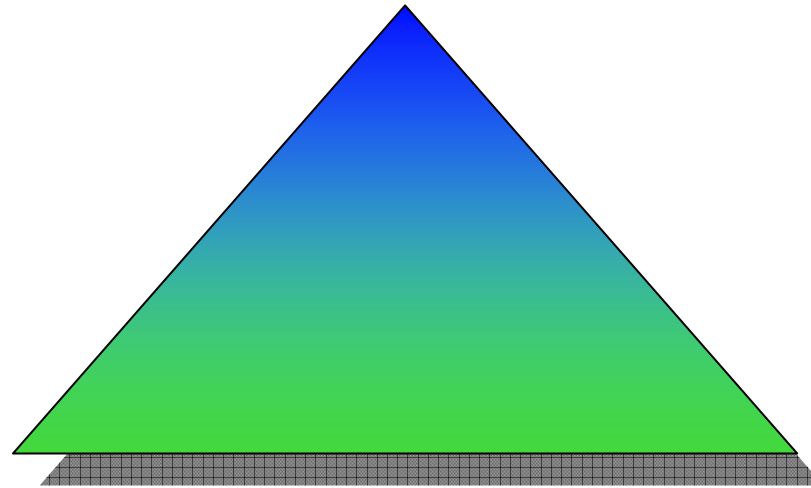
High Speed Design is the study of analog effects on Timing



- Component timing (process)
- Voltage
- Temperature
- Package & PCB routing lengths
- PCB manufacturing variations (Z_0 , loss)
- Reflection/Overshoot
- ISI
- SSN/SSO
- Crosstalk...

High Speed Design

Constraint-Driven Design



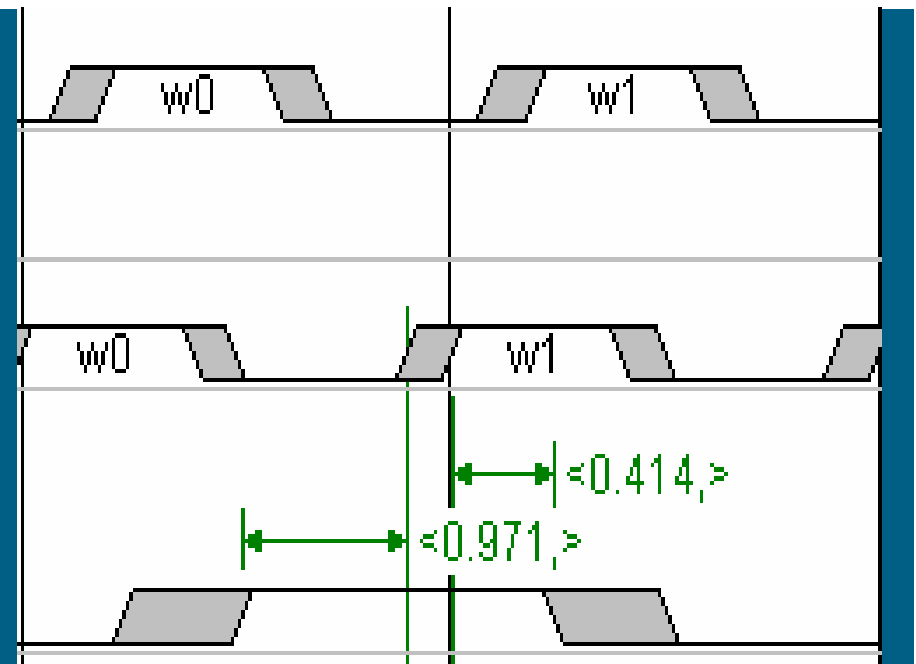
Static Timing Analysis

Signal & Power
Integrity Analysis

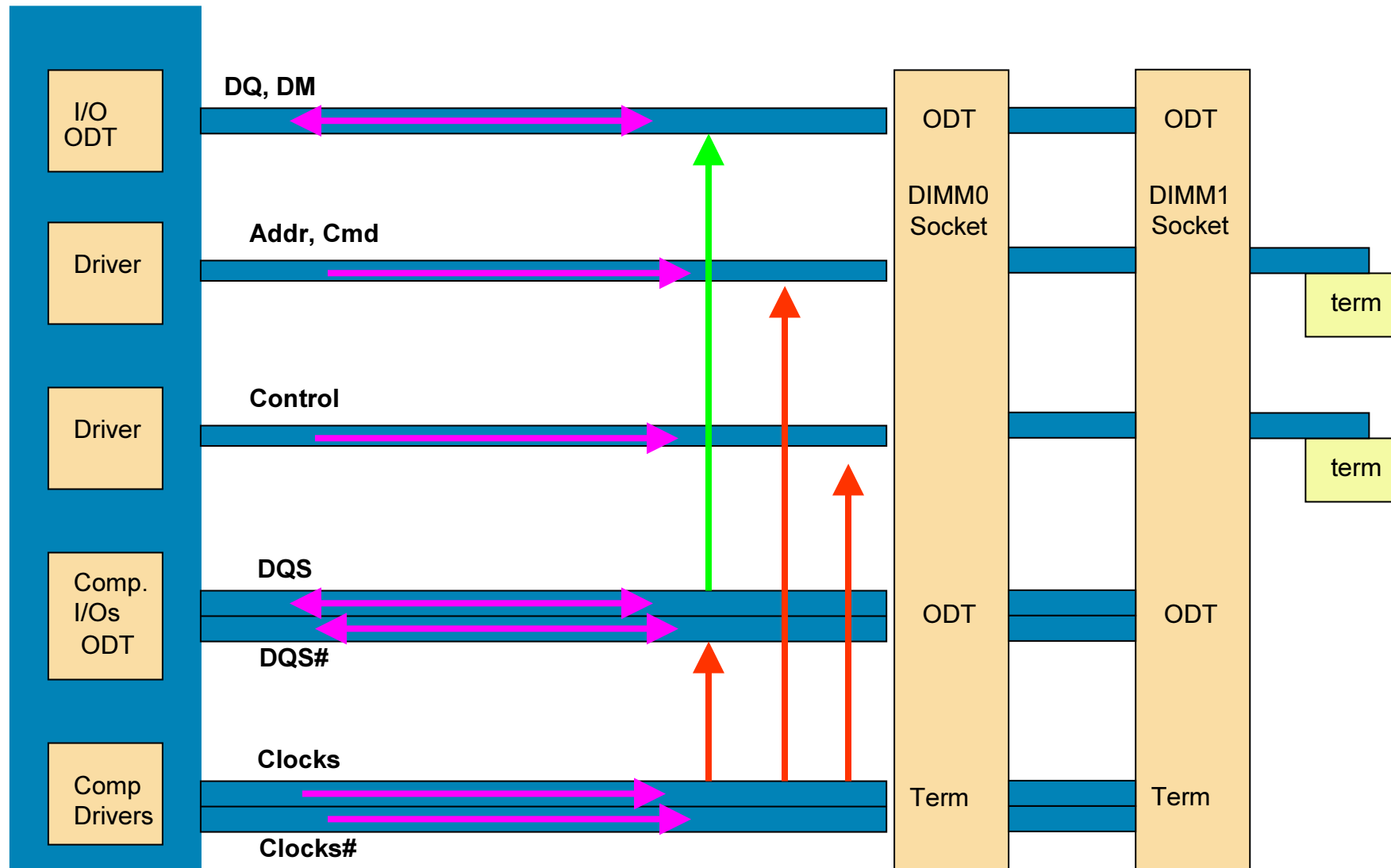
Audience Poll #1

What is the fastest memory design you have worked on ?	
	Votes
Less than 200MHz	
DDR2 400-533 Mts	
DDR2 667-800 Mts	
DDR3 800-1066 Mts	
DDR3 1333-1600 Mts	
No Active design	

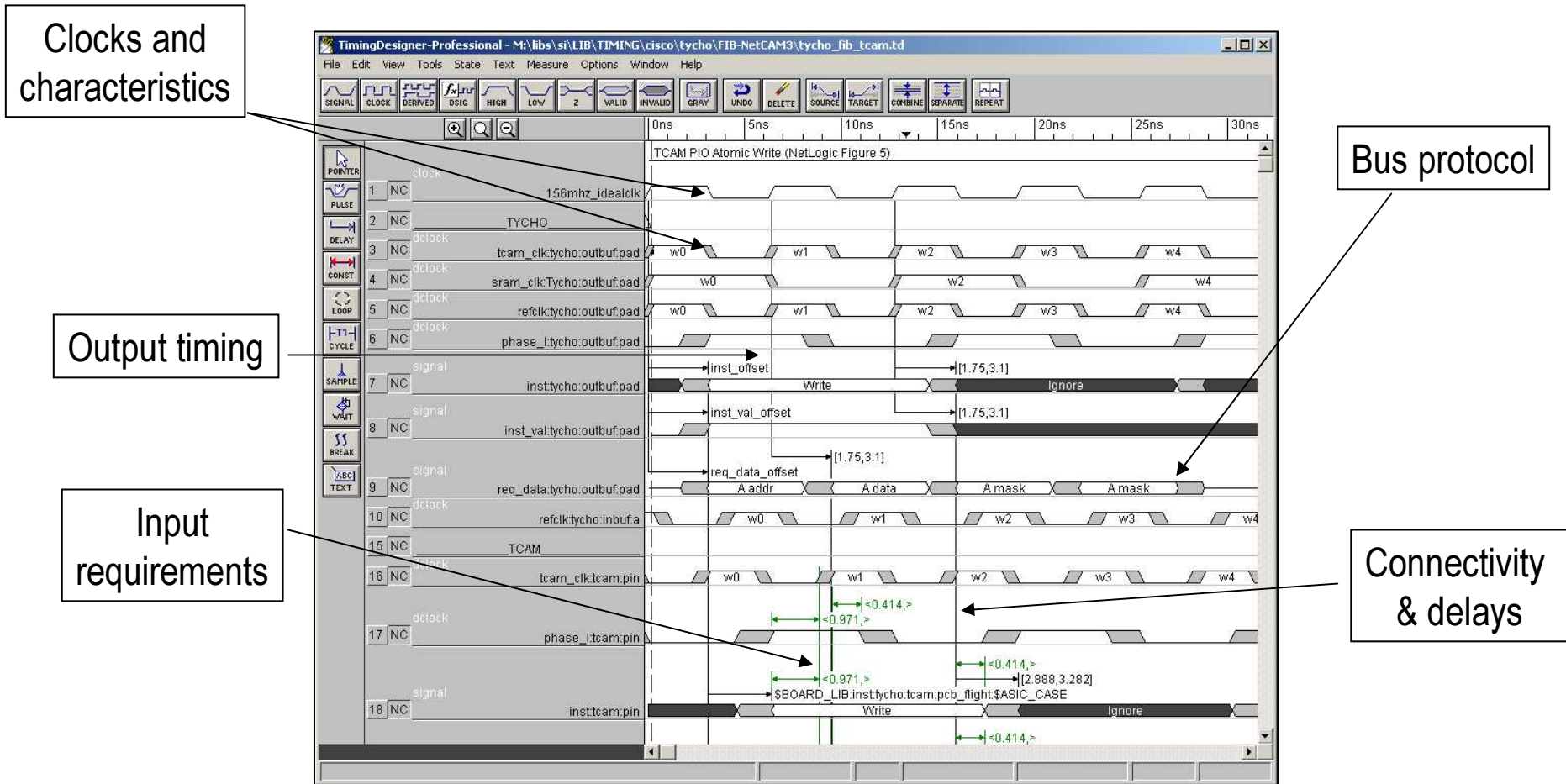
Static Timing Analysis



Timing Budget for DDR2



Develop a Static Timing Model



STA for DDR2 is based on vendors datasheet (which are JESD79-2C based)



256Mb: x4, x8, x16 DDR2 SDRAM AC Operating Specifications

Table 48: AC Operating Conditions for -3E, -3, -37E and -5E Speeds (Sheet 4 of 6)

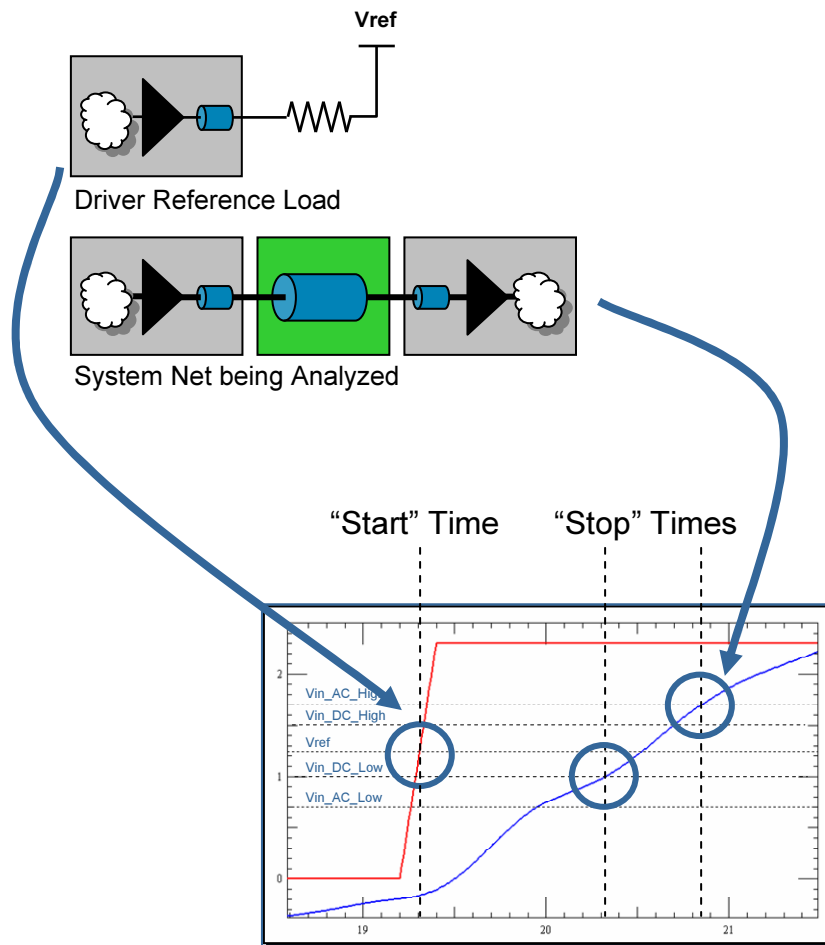
Notes: 1-5; notes appear on page 125; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC Characteristics		-3E		-3		-37E		-5E		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Address and control input pulse width for each input	t_{IPW}	0.6		0.6		0.6		0.6		t_{CK}	37
Address and control input setup time	t_{IS_a}	400		400		500		600		ps	6, 19
Address and control input hold time	t_{IH_a}	400		400		500		600		ps	6, 19
Address and control input setup time	t_{IS_b}	200		200		250		350		ps	6, 19
Address and control input hold time	t_{IH_b}	275		275		375		475		ps	6, 19

DDR2 Timing

- Data Sheet Timing is with respect to a specific load
 - Reference: 25 ohms to VDDQ/2
 - Timing measured to Vref
- Device timing is measured with respect to thresholds
 - Dependant on operating frequency
 - IO type used (DM_INPUT_533/DQFULL_533, INPUT_533(ADDR))
 - Specific edge (Rising, Falling)
 - Slew rates of the signals

Data Sheet Timing and Interconnect Delays



- Interconnect delays from simulations have *start* and *stop* times

Start times are based on output timing specs

Reference loads and voltage levels

IBIS V_{ref} , C_{ref} , R_{ref} , V_{meas}

Stop times are based on input (setup/hold) timing specs

Measured at defined voltage levels and slew rates

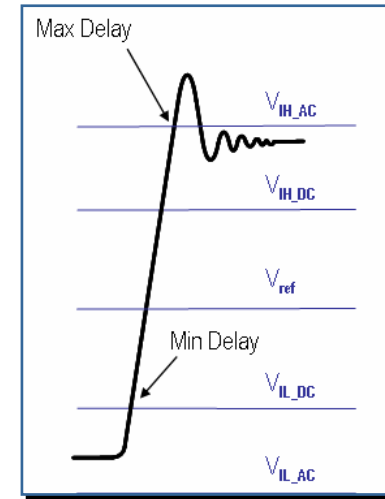


Device timing (DQ Signals)

Note: Guard bands not shown

Quality

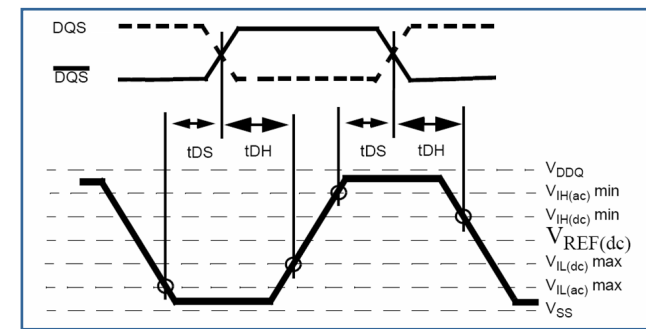
- A rising edge must:
 - Start below V_{IL_DC}
 - Switch through V_{IH_AC}
 - Settle above V_{IH_DC}



SI View

Timing

- **MIN** delay measured at first crossing of V_{IL_DC}
 - Used to compute hold margin
 - JESD79-2C, page 96, note 21
- **MAX** delay measured at first crossing of V_{IH_AC}
 - Used to compute setup margin
 - JESD79-2C, page 96, note 20



Timing Spec View

Timing files to implement STA

667 DDR2 parts running at 667 DDR2

ADDCMD_SETUP = 0.200

ADDCMD_HOLD = 0.275

CTRL_SETUP = 0.200

CTRL_HOLD = 0.275

DQ_SETUP = 0.100

DQ_HOLD = 0.175

tQHS_SKEW_MAX = 0.340

tDQSQ_SKEW_MAX = 0.240

#DQ Write timing

SETHLD DQ *TO R DQS DQ_SETUP

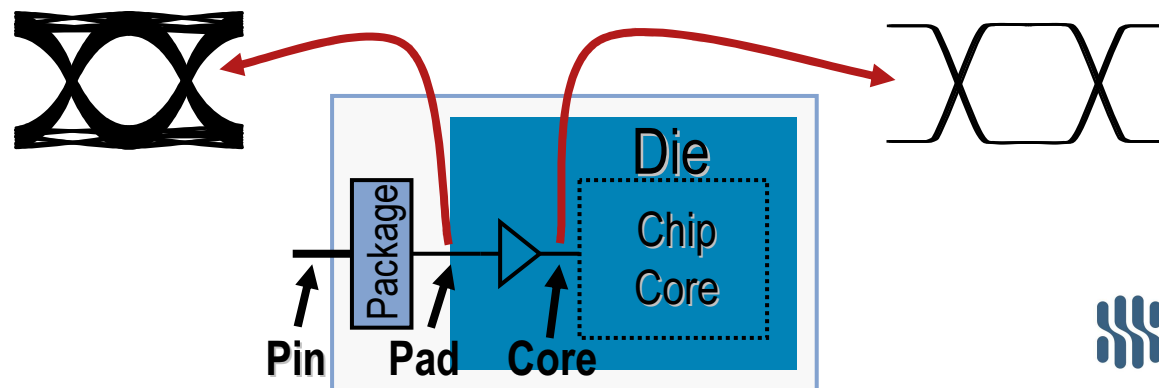
DQ_HOLD

SETHLD DQ *TO F DQS DQ_SETUP

DQ_HOLD

DDR2 Slew Rate Derating

- Baseline setup/hold requirements are based on specific voltage and slew rate conditions
- System slew rates rarely conform to measurement conditions
Loading can vary widely within the same system
- DDR2 slew-rate derating defines adjustments to setup/hold specs based on actual slew rates of input signals



SiSoft's Slew Rate Methodology

- Device setup/hold times based on nominal (base) values
- Derating tables converted into independent derating values for DQ and DQS nets
- Derating info included in simulation models – measurements & adjustments are automated

DQ Vref->AC Slew Rate |SiSoft_Derate_Max

DQ DC->Vref Slew Rate -|SiSoft_Derate_Min

Table 29: DDR2-667 ¹DS, ¹DH Derating Values with Differential Strobe
Notes: 1-7: all units in ps

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate																	
	2.8 V/ns		2.4 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	Δ^1 DS	Δ^1 DH	Δ^1 DS	Δ^1 DH	Δ^1 DS	Δ^1 DH	Δ^1 DS	Δ^1 DH	Δ^1 DS	Δ^1 DH	Δ^1 DS	Δ^1 DH	Δ^1 DS	Δ^1 DH	Δ^1 DS	Δ^1 DH	Δ^1 DS	Δ^1 DH
2.0	100	63	100	63	100	63	112	75	124	87	136	99	148	111	160	123	172	135
1.5	67	42	67	42	67	42	79	54	91	66	103	78	115	90	127	102	139	114
1.0	0	0	0	0	0	0	12	12	24	24	36	36	48	48	60	60	72	72
0.9	-5	-14	-5	-14	-5	-14	7	-2	19	10	31	22	43	34	55	46	67	58
0.8	-13	-31	-13	-31	-13	-31	-1	-13	11	-7	23	5	35	17	47	29	59	41
0.7	-22	-54	-22	-54	-22	-54	-10	-42	2	-30	14	-18	26	-6	38	6	50	18
0.6	-34	-83	-34	-83	-34	-83	-22	-71	-10	-59	2	-47	14	-35	26	-23	38	-11
0.5	-60	-125	-60	-125	-60	-125	-48	-113	-36	-101	-24	-89	-12	-77	0	-65	12	-53
0.4	-100	-188	-100	-188	-100	-188	-88	-176	-76	-164	-64	-152	-52	-140	-40	-128	-28	-116

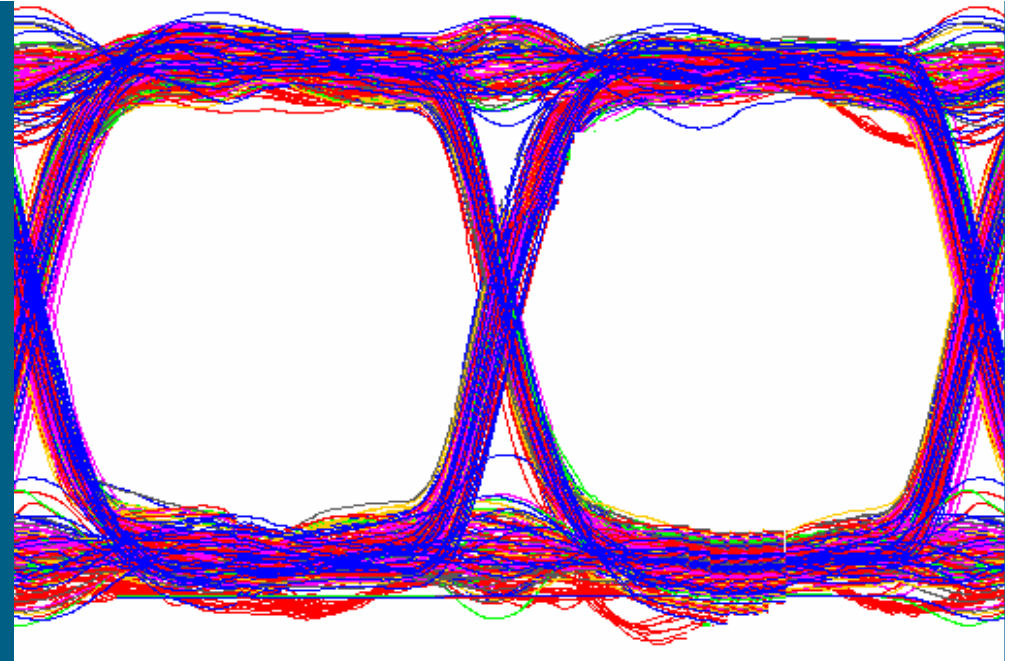
DQS DC->AC Slew Rate |SiSoft_Derate_Max

DQS DC->AC Slew Rate -|SiSoft_Derate_Min

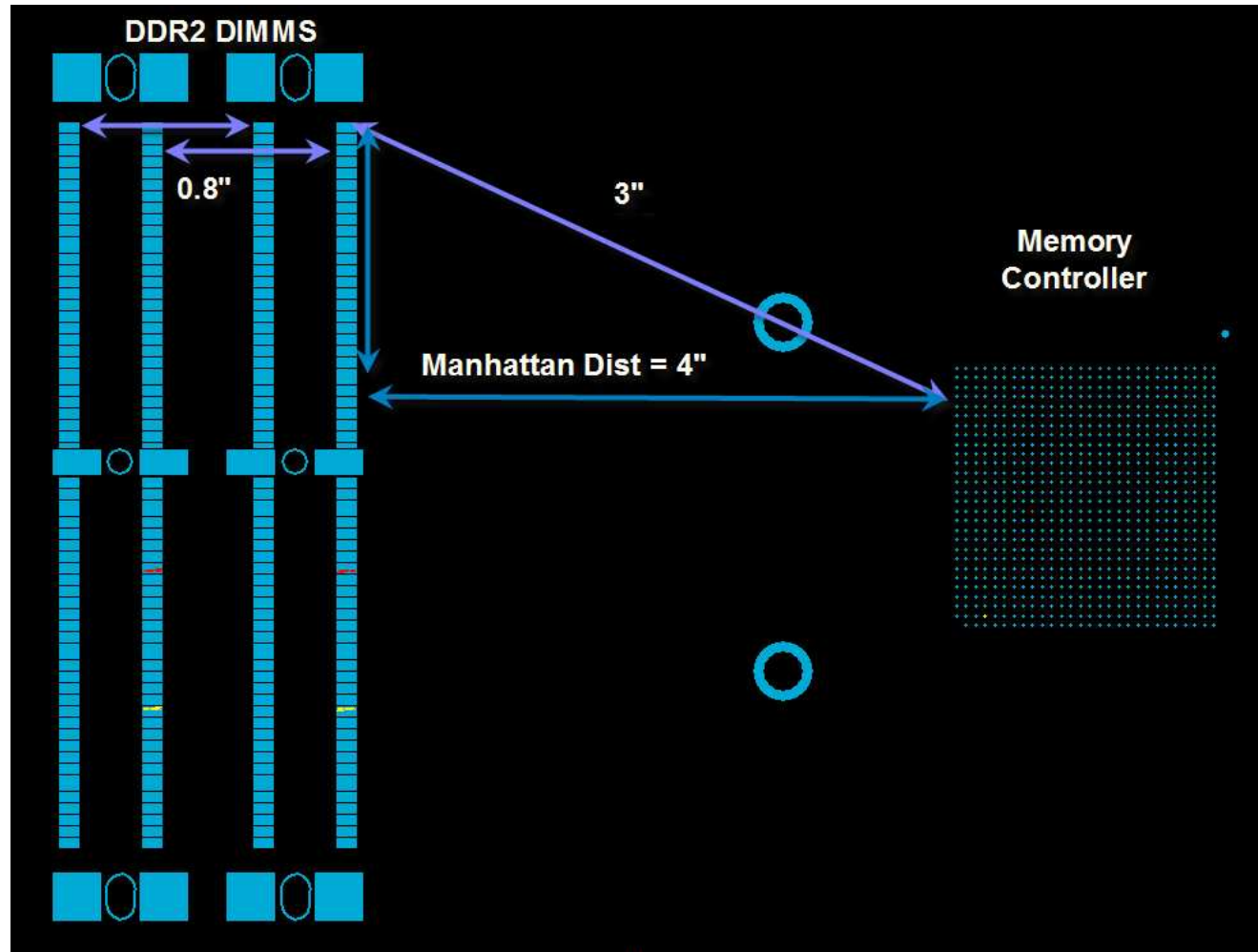
Nominal slew rate row and column



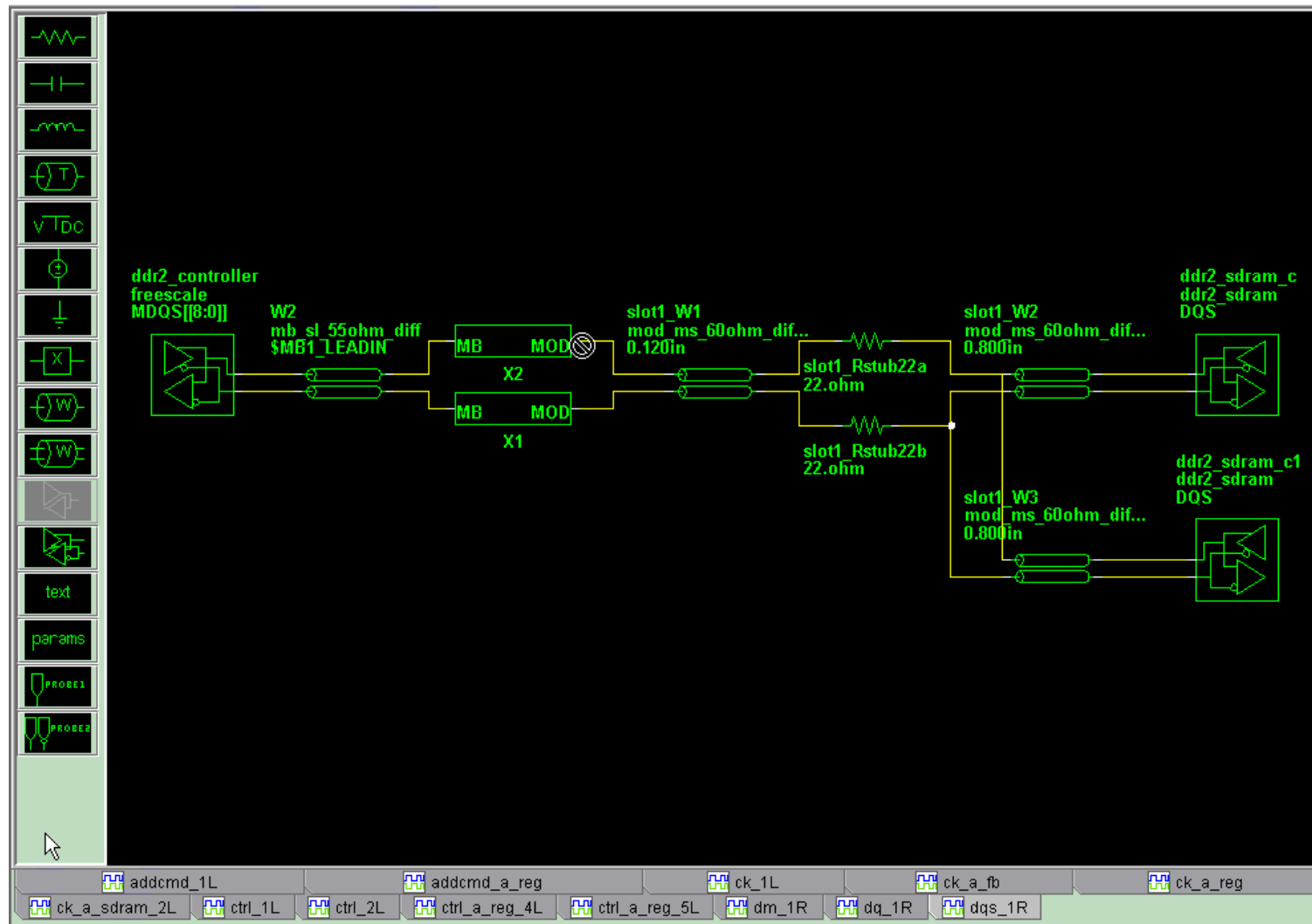
Pre-route simulations



PCB component placement



Topologies for current placement



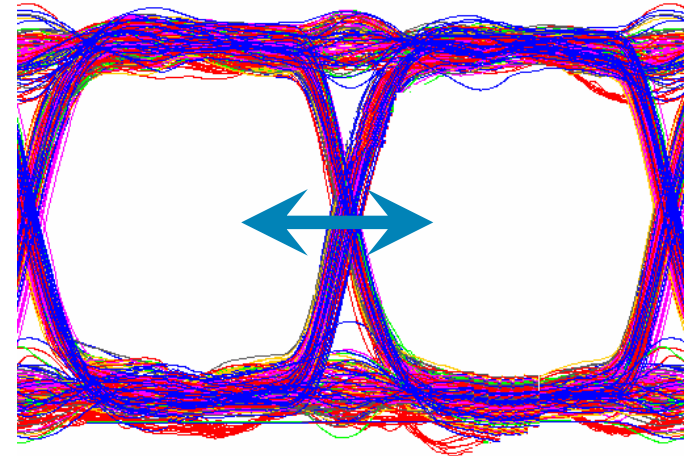
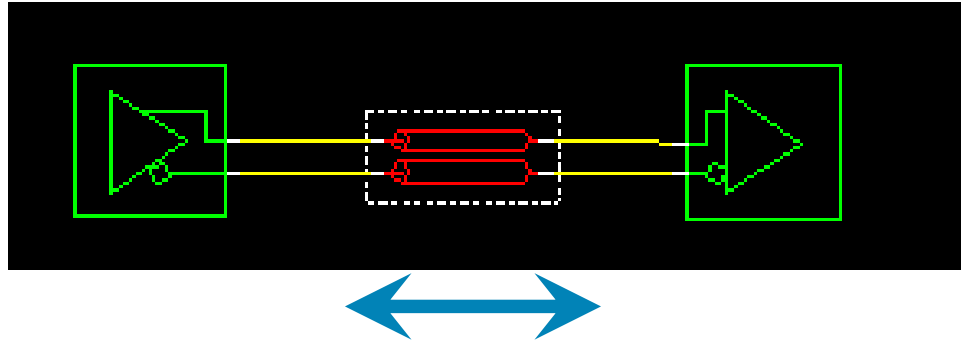
Extracted Topologies add sweep variables for Cad constraints, and select ODT settings

The screenshot displays a circuit simulation environment. On the left is a toolbar with various components like resistors, capacitors, inductors, and transmission lines. The main workspace shows a circuit diagram with a PLL component (ddr2_pll) connected to several transmission line models (WTL0, WTL1, WTL2, WTL3a, WTL3b, WTL3b1, WTL3b2) which are in turn connected to four SDRAM components (ddr2_sdram_1, ddr2_sdram_2, ddr2_sdram_3, ddr2_sdram_4). The transmission lines are labeled with 'mod_ms_60ohm_diff' and variables like '\$TL0' through '\$TL3'. A resistor component (R1) is also visible.

Below the workspace is a 'Solution Space' table with the following data:

Transfer Net	Variable:	Type:	Variation Group:	Value 1:	Value 2:
ck_a_reg	\$TL0	W Length	length	\$G_A_CK_REG_TL0	\$G_A_CK_REG_TL0
ck_a_reg	\$TL1	W Length	length	\$G_A_CK_REG_TL1	\$G_A_CK_REG_TL1
ck_a_reg	\$TL2	W Length	length	\$G_A_CK_REG_TL2	\$G_A_CK_REG_TL2
ck_a_sdram_2L	\$R1	Resistance	term r	\$G_A_CK_SDRAM_R1	\$G_A_CK_SDRAM_R1
ck_a_sdram_2L	\$TL0	W Length	length	\$G_A_CK_SDRAM_TL0	\$G_A_CK_SDRAM_TL0
ck_a_sdram_2L	\$TL1	W Length	length	\$G_A_CK_SDRAM_TL1	\$G_A_CK_SDRAM_TL1
ck_a_sdram_2L	\$TL2	W Length	length	\$G_A_CK_SDRAM_TL2	\$G_A_CK_SDRAM_TL2
ck_a_sdram_2L	\$TL3	W Length	length	\$G_A_CK_SDRAM_TL3	\$G_A_CK_SDRAM_TL3

Scanning the design space

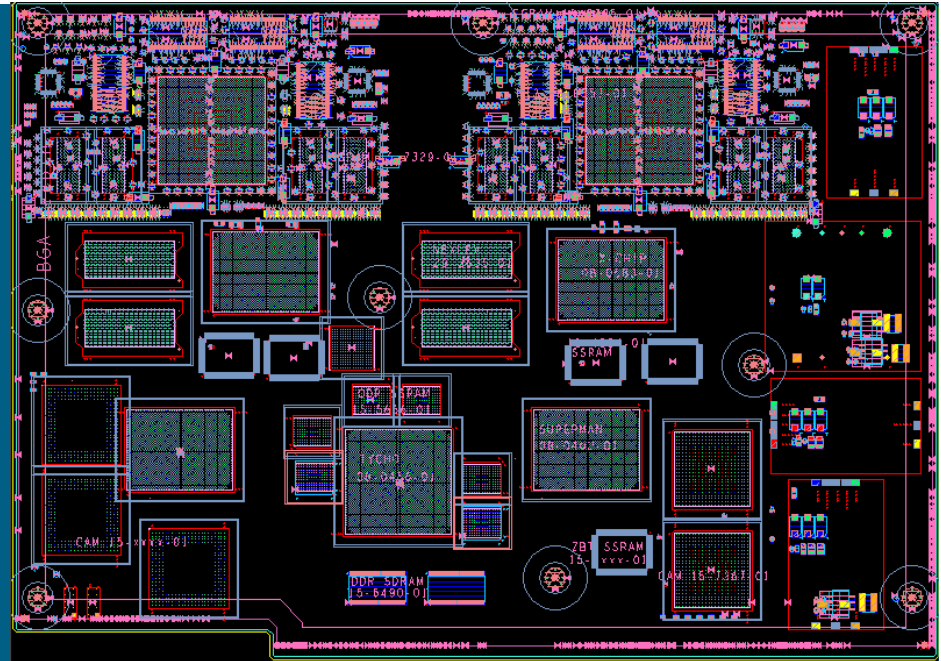


- Sweep topology from 2 inches to 3 inches
- How does this change the timing? TOF [400ps, 600ps]
- Allowable tolerance = +/- 500 ?
- Well 😊

Verify the pre-route timing across case

Setup Margin (ns)	Hold Margin (ns)	Rmin Etch Delay (ns)	Rmax Etch Delay (ns)	Fmin Etch Delay (ns)	Fmax Etch Delay (ns)	Transfer Net
0.037	0.784	1.331	1.71	1.331	1.71	DQS_ECC_2R_2Slot
0.153	0.585	1.206	1.616	1.205	1.614	DQS_2R_2Slot
0.828	1.01	1.037	1.511	1.072	1.412	Pre_reg_cmd_slot1
0.807	1.03	1.153	1.675	1.189	1.575	Pre_reg_cmd_slot2
0.375	1.127	1.154	1.907	1.195	1.748	Pre_reg_CS
0.617	1.006	1.033	1.865	1.067	1.744	Pre_reg_addcmd
0.344	0.232	1.132	1.795	1.143	1.741	DQ_2R_2Slot
0.395	0.305	1.293	1.662	1.294	1.603	DM_2R_2Slot
1.223	1.411	0.827	1.244	0.771	1.312	Post_reg_addcmd_LB
1.169	1.255	0.756	1.34	0.623	1.376	Post_reg_addcmd_RB
1.442	1.228	0.701	1.091	0.615	1.08	Post_Reg_CTRL_4L
0.875	1.356	0.819	1.592	0.733	1.656	Post_Reg_CTRL_5L

Routing Rules Development for CAD



Audience Poll #2

- How do the rules get into your designs?

Cad engineer enters them

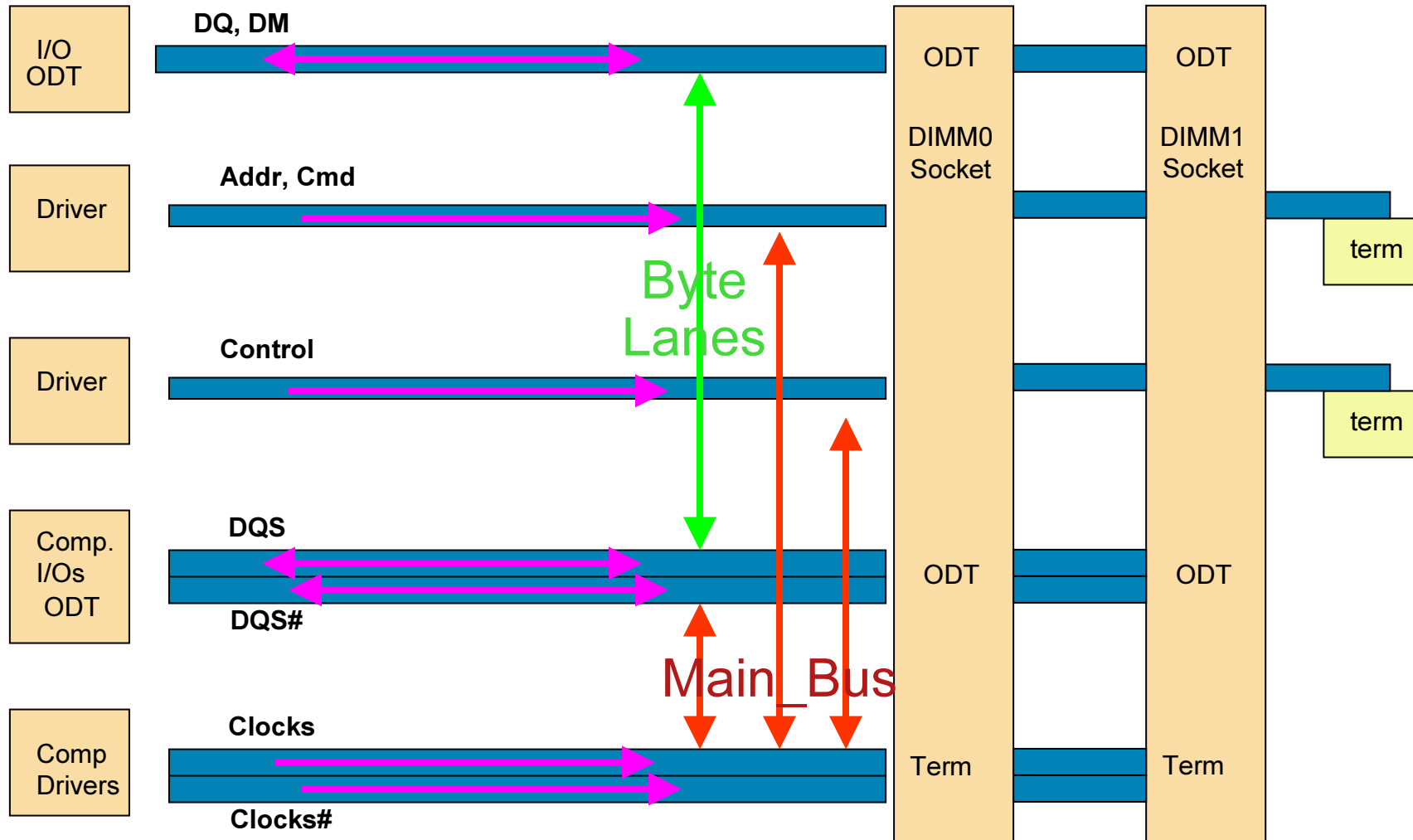
HW Engineering enters them in the cad tool

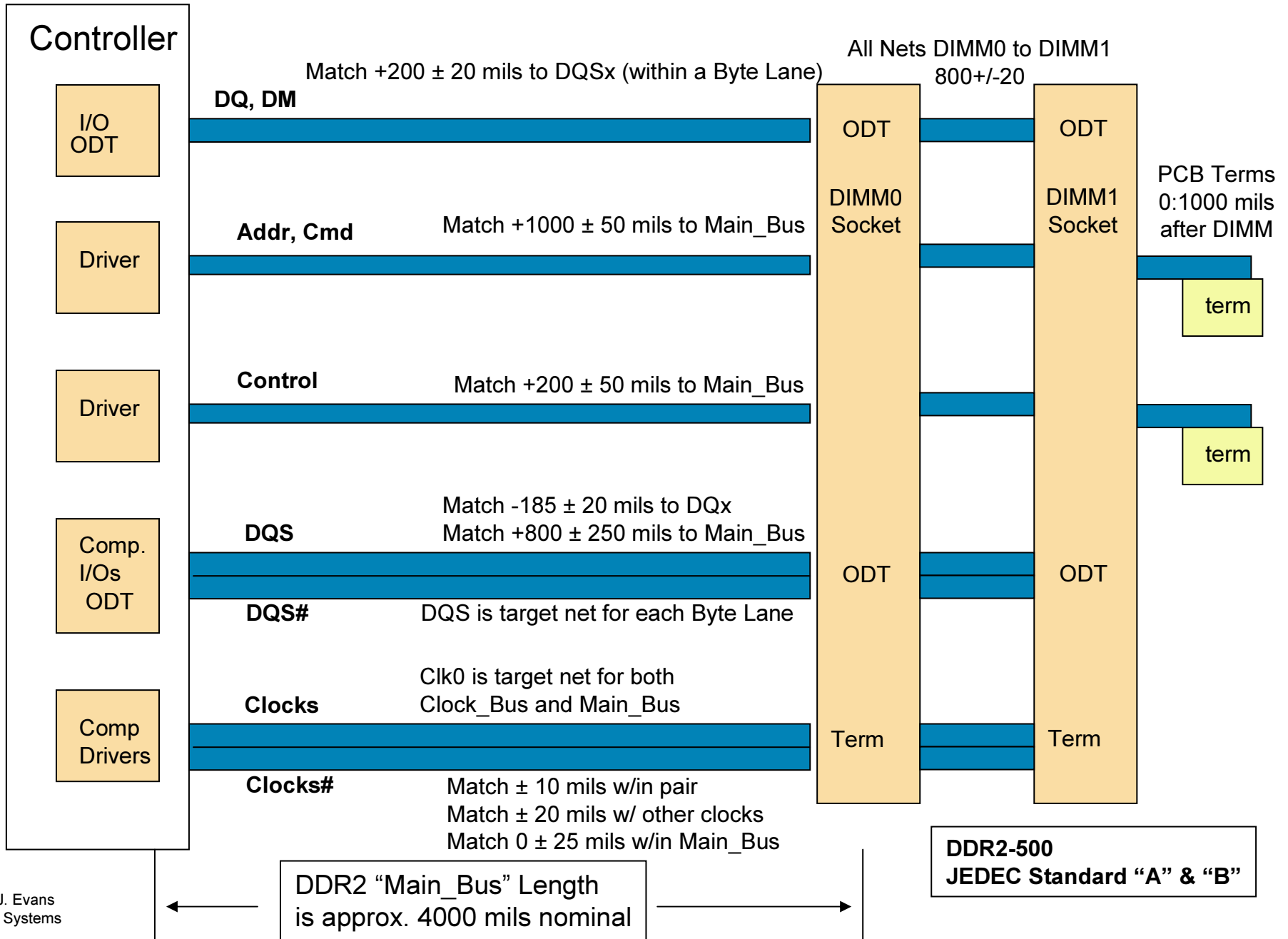
Rules flow in from the schematic from HW

Added via 3rd party tool (Cad or HW)

Other Methods?

Define rule sets to meet Timing





Rules in Allegro CMS

The screenshot shows the Allegro Constraint Manager interface. On the left is a tree view of constraint sets, including 'Electrical Constraint Set', 'Net', and 'DRC'. The main area displays a table of rules for 'Relative Propagation Delay'.

Objects	Reference	Pin Pair	Pin Delay		Scope	Relative Delay			
			Pin 1 mil	Pin 2 mil		Delta:Tolerance ns	Actual	Margin	
RP_DATA_BUS								0.23 MIL	
RP_DATA_LANE_0								9.93 MIL	
RP_DATA_LANE_1								1.65 MIL	
U1U.F3:J3D.143 [MEM_D15]					Global	185 MIL:10 MIL		0.07 MIL	9.93 MIL
U1U.F6:J3D.22 [MEM_D11]					Global	185 MIL:10 MIL		3.02 MIL	6.98 MIL
U1U.G4:J3D.142 [MEM_D14]					Global	185 MIL:10 MIL		6.27 MIL	3.73 MIL
U1U.G5:J3D.21 [MEM_D10]					Global	185 MIL:10 MIL		0.53 MIL	9.47 MIL
U1U.H1:J3D.16 [MEM_DQS]					Global	:0 MIL		TARGET	
U1U.H3:J3D.15 [MEM_DQS]					Global	0 MIL:10 MIL		0.41 MIL	9.59 MIL
U1U.H4:J3D.136 [MEM_DM]					Global	185 MIL:10 MIL		5.12 MIL	4.88 MIL
U1U.J5:J3D.134 [MEM_D13]					Global	185 MIL:10 MIL		0.79 MIL	9.21 MIL
U1U.J6:J3D.13 [MEM_D9]					Global	185 MIL:10 MIL		8.35 MIL	1.65 MIL
U1U.K4:J3D.12 [MEM_D8]					Global	185 MIL:10 MIL		1.53 MIL	8.47 MIL
U1U.K5:J3D.133 [MEM_D12]					Global	185 MIL:10 MIL		0.3 MIL	9.7 MIL
RP_DATA_LANE_2									0.09 MIL
RP_DATA_LANE_3									3.51 MIL
RP_DATA_LANE_4									1.83 MIL
RP_DATA_LANE_5									2.41 MIL
RP_DATA_LANE_6									3.22 MIL
RP_DATA_LANE_7									0.14 MIL
RP_DATA_LANE_8									0.19 MIL
RP_DDR2_CLOCKS_FAR									2.49 MIL

At the bottom of the window, there are buttons for 'SYNC' and 'XNET', and a status bar with the text 'Click and drag to change column size'.

Why do we often over constrain designs?

- Fear of design failure
- Leveraged rules from working revision
- Application note requirements
- Lack of a HSD support
- Tighter must be better
- Automated rules generation

Dk Based Time to Length Conversion

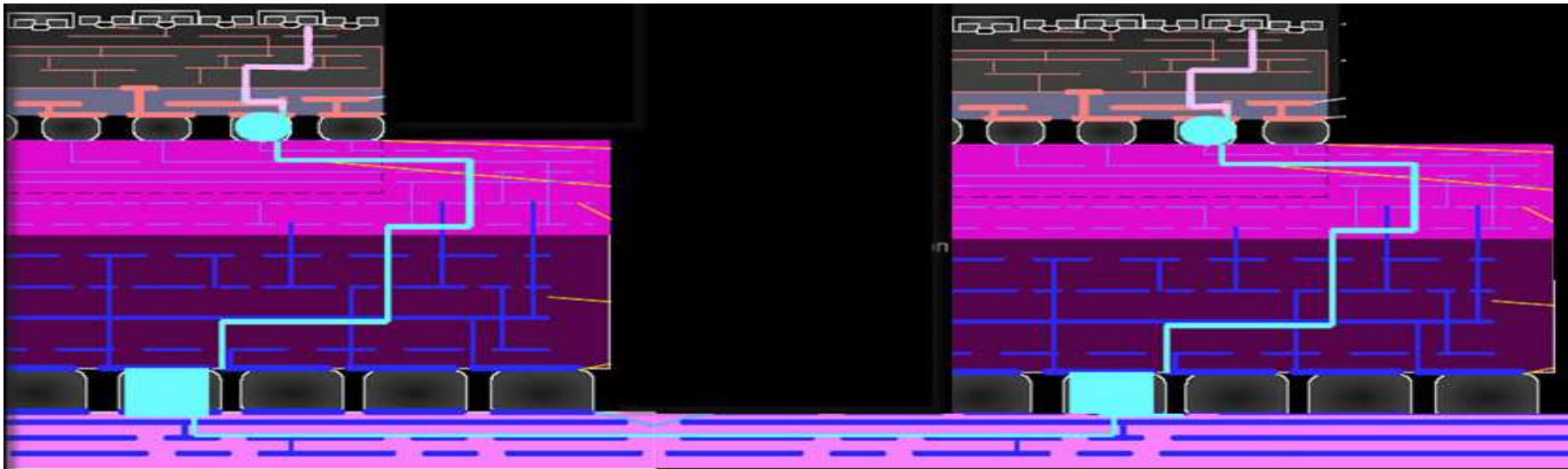
Time (ps) $\epsilon_r \sim 4.5$	Length (mills)
180	1000
18	100
1.8	10
0.18	1

Layer 5 routing, 4"
-> 720 pS

Time (ps) $\epsilon_r \sim 3.2$	Length (mills)
150	1000
15	100
1.5	10
0.15	1

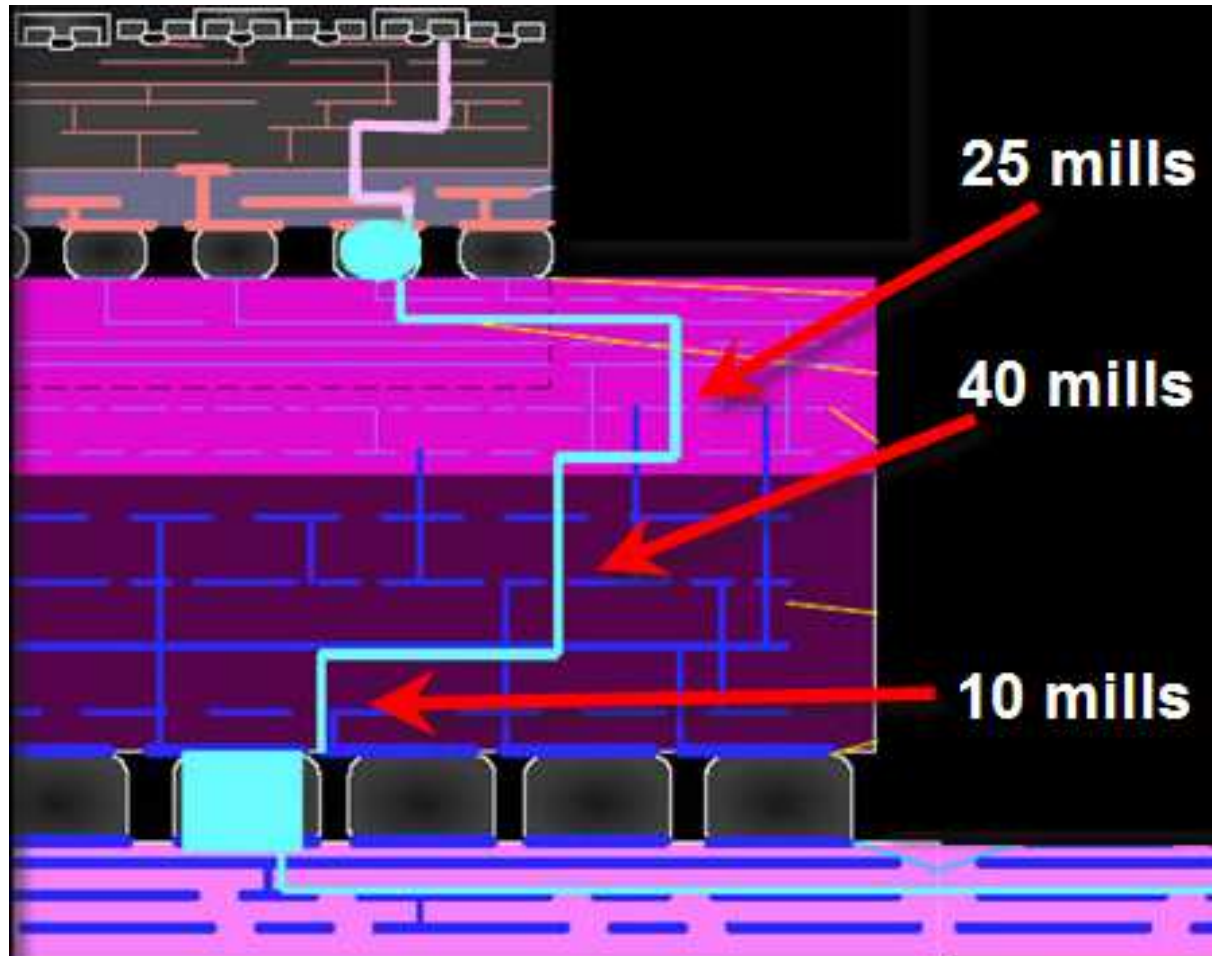
Layer 12 routing, 4"
-> 600 pS

Pin Delay Info



Objects	Reference	Pin Pairs	Pin Delay		Prop Delay			Prop Delay		
			Pin 1	Pin 2	Min	Actual	Margin	Max	Actual	Margin
			mil	mil	ns			ns		
[-] QDR_NPU1_QDR_STM_ADDR11										
								1000 MIL		
								1000 MIL		
								4500 MIL		
[-] QDR_NPU1_QDR_STM_ADDR12										
								1000 MIL		
								1000 MIL		
								4500 MIL		

What adds up in the path Length ?



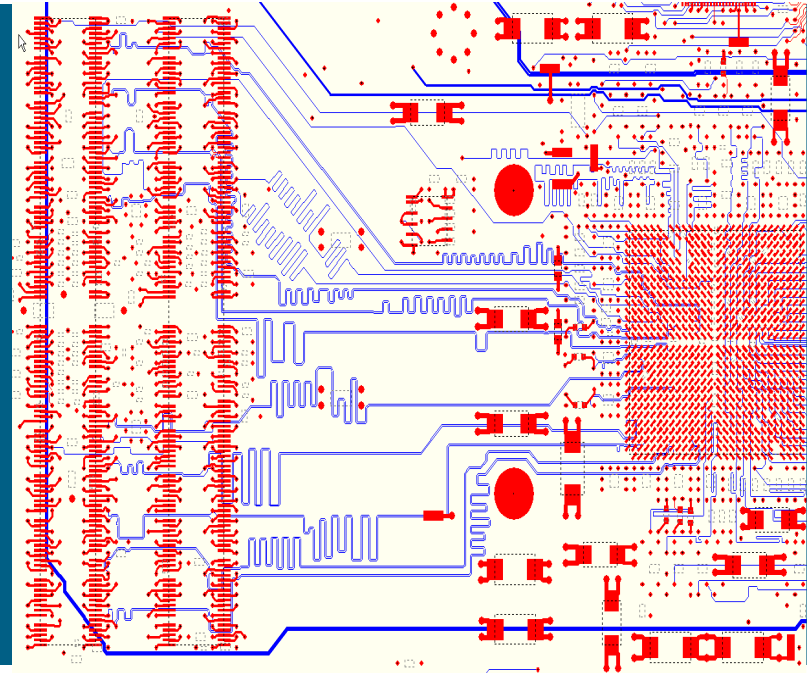
Audience Quiz: Via delay

- We have an match for 2 nets.
- Each has the exact same etch

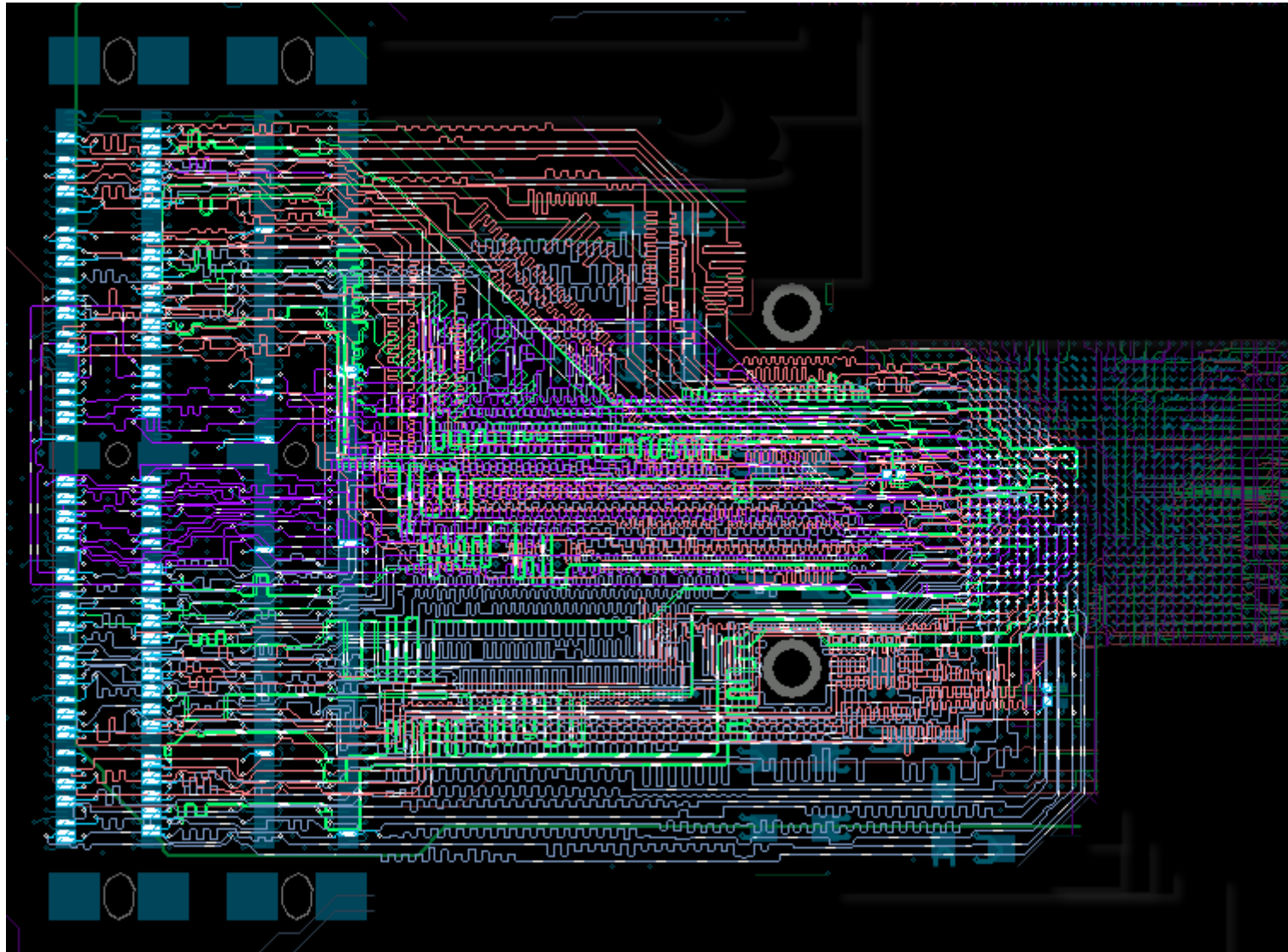
What is the diff in the CMS tool ?

	Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent
1		SURFACE	AIR				
2	TOP	CONDUCTOR	PLATED_COPPER_FOIL	2.4	343000	4.50000	
3		DIELECTRIC	FR-4	3.73	595900	3.70000	0.035
4	P02_1P1	PLANE	COPPER				
5		DIELECTRIC	FR-4				0.035
6	G03	PLANE	COPPER				
7		DIELECTRIC	FR-4	3.73	595900	3.70000	0.035
8	T04	PLANE	COPPER	0.65	595900	4.50000	0
9		DIELECTRIC	FR-4	4.3	595900	3.670000	0.035
10	T05	PLANE	COPPER	0.65			
11		DIELECTRIC					
12	G06	PLANE		82 mills		82 mills	
13		DIELECTRIC			595900	3.800000	0.035
14	T07	CONDUCTOR	COPPER	0.65	595900	4.500000	0
15		DIELECTRIC	FR-4	5.4	595900	3.710000	0.035
16	T08	CONDUCTOR	COPPER	0.65	595900	4.500000	0
17		DIELECTRIC	FR-4	3.5	595900	3.800000	0.035
18	G09	PLANE	COPPER	1.3	595900	4.500000	0
19		DIELECTRIC	FR-4	3.73	595900	3.700000	0.035
20	T10	CONDUCTOR	COPPER	0.65	595900	4.500000	0
21		DIELECTRIC	FR-4	4.3	595900	3.670000	0.035
22	T11	CONDUCTOR	COPPER	0.65	595900	4.500000	0
23		DIELECTRIC	FR-4	3.73	595900	3.700000	0.035
24	G12	PLANE	COPPER	1.3	595900	4.500000	0
25		DIELECTRIC	FR-4	2	595900	4.400000	0.035
26	P13_3P3	PLANE	COPPER	1.3	595900	4.500000	0
27		DIELECTRIC	FR-4	6.1	595900	3.800000	0.035
28	P14_2P5	PLANE	COPPER	1.3	595900	4.500000	0
29		DIELECTRIC	FR-4	2	595900	3.800000	0.035
30	G15	PLANE	COPPER	1.3	595900	4.500000	0
31		DIELECTRIC	FR-4	3.73	595900	3.700000	0.035
32	T16	CONDUCTOR	COPPER	0.65	595900	4.500000	0
33		DIELECTRIC	FR-4	4.3	595900	3.670000	0.035
34	T17	CONDUCTOR	COPPER	0.65	595900	4.500000	0
35		DIELECTRIC	FR-4	3.73	595900	3.700000	0.035
36	G18	PLANE	COPPER	1.3	595900	4.500000	0
37		DIELECTRIC	FR-4	3.5	595900	3.800000	0.035

Post Route Simulations



Fully routed Allegro design



QSI for Post Route Simulations

Extended Net Simulation

Available: 3751

Included: 175

Xtalk Scan Violations Only

Simulation Mode

SI/Timing

Crosstalk

Incremental

Post-Layout Operations

Transfer Net	Pin Equivalent Net	Extended Net	Simulate	Simulation Status	Simulate Incrementally	Data Rate	Type	Mode	Coupling Type	Crosstalk Group
addcmd_1L	2p_1o_1i_A_1u	rp_base%DDR_CAS_L	Yes	Unsimulated	No	5.0ns	Data	Single Ended	Sync	addcmd_1L
addcmd_1L	2p_1o_1i_A_1u	rp_base%DDR_MA[13:0]	Yes	Unsimulated	No	5.0ns	Data	Single Ended	Sync	addcmd_1L
addcmd_1L	2p_1o_1i_A_1u	rp_base%DDR_MBA[2:0]	Yes	Unsimulated	No	5.0ns	Data	Single Ended	Sync	addcmd_1L
addcmd_1L	2p_1								Sync	addcmd_1L
addcmd_1L	2p_1								Sync	addcmd_1L

Post-Layout Simulation Control

Corners:

Etch

SE TE FE

SS

IC TT

FF

State:

Drivers:

Receivers:

AC Noise:

Reference Schematic Overrides:

Use for Drivers & Receivers

Use for Corners

Simulation Control

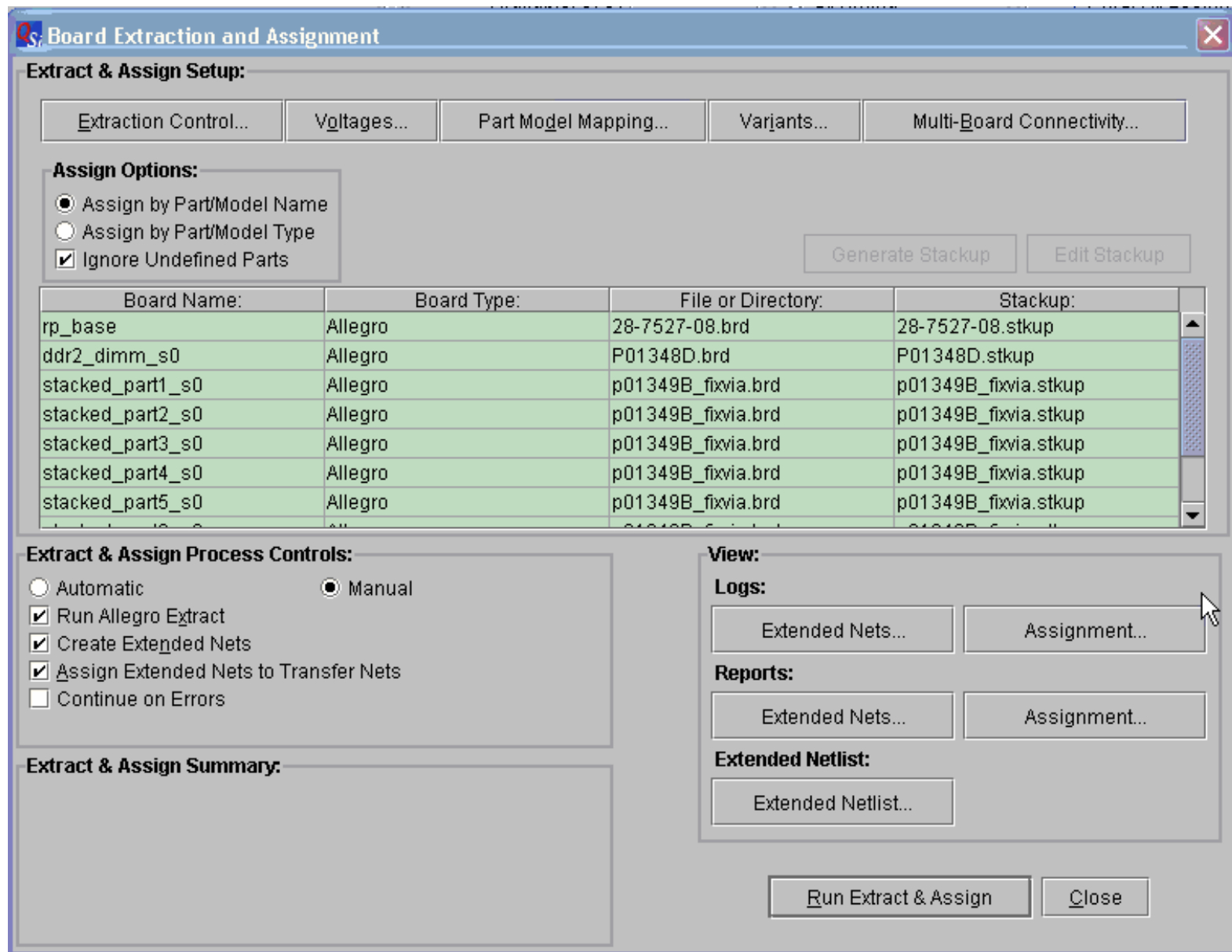
Default AC Noise:

Transfer Net	State	AC Noise Source	AC Noise
addcmd_1L	A	Transfer Net	+/-0.0V
addcmd_a_reg	default	Transfer Net	+/-0.00V
ck_1L	A	Transfer Net	+/-0.0V
ck_a_fb	default	Transfer Net	+/-0.00V
ck_a_reg	default	Transfer Net	+/-0.00V
ck_a_sdrum_2L	default	Transfer Net	+/-0.00V
ctrl_1L	A	Transfer Net	+/-0.0V
ctrl_2L	default	Transfer Net	+/-0.00V
ctrl_a_reg_4L	default	Transfer Net	+/-0.00V
ctrl_a_reg_5L	default	Transfer Net	+/-0.00V
dm_1R	A	Transfer Net	+/-0.0V
dq_1R	A	Transfer Net	+/-0.0V
dqs_1R	A	Transfer Net	+/-0.0V

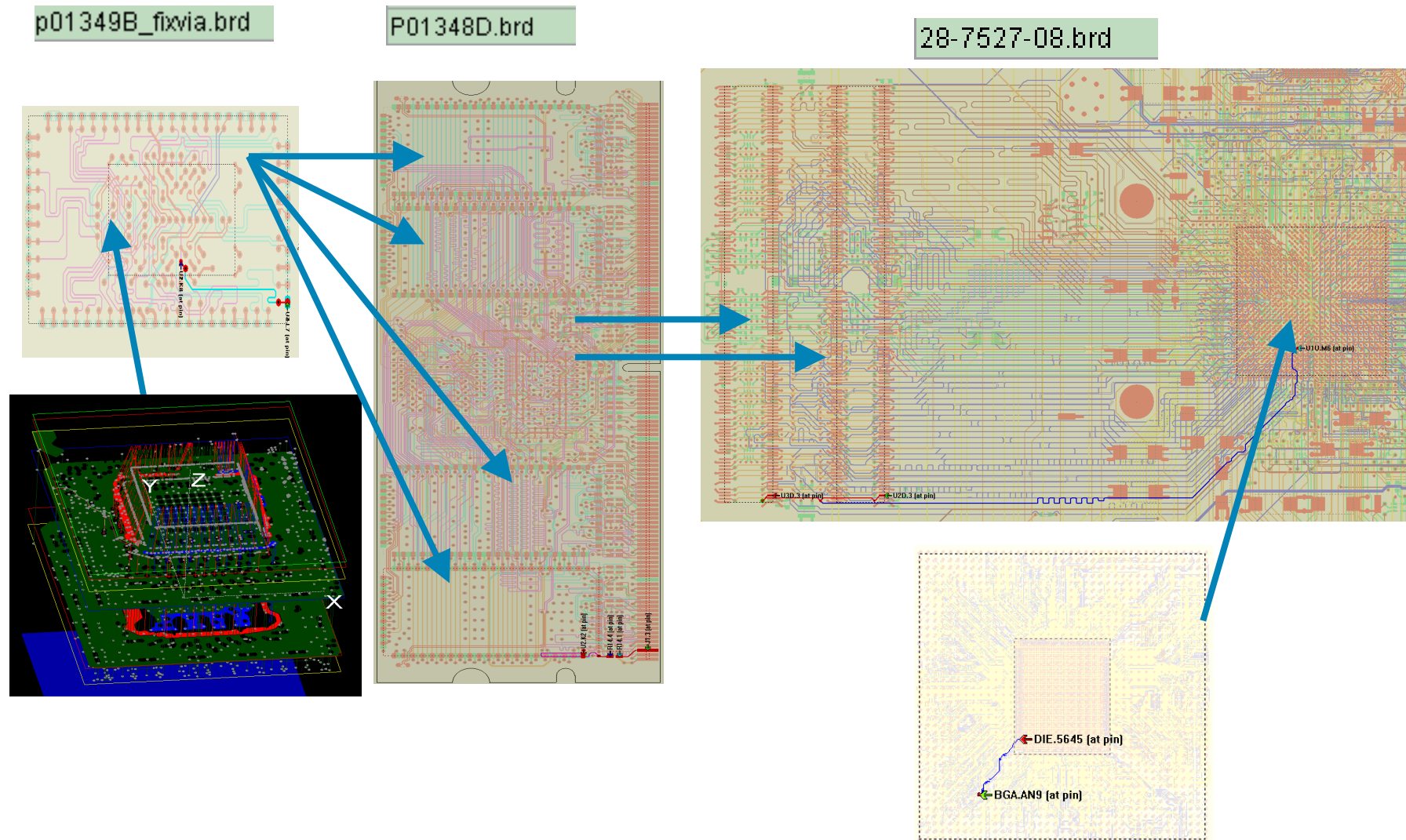
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Multi Board Extractions with QSI



Multi Board Extractions with QSI



Transfer Nets in QSI

Transfer Net Properties

Transfer Nets:

Transfer Net	Clock Domain	Data Rate	Switching Frequency	Type	Mode	Source Probe Points	Target Probe Points	Jitter	Uncorrelate Etch Facto
dm_1R	ddr2_dq_rate	2.5ns	400.0MHz	Data	Single_Ended	SL_pad	pad	N/A	
dq_1R	ddr2_dq_rate	2.5ns	400.0MHz	Data	Single_Ended	SL_pad	pad	N/A	
dqs_1R	ddr2_dqs_rate	2.5ns	400.0MHz	Strobe	Differential	SL_pad	pad	0	

Nodes:

Designator	Subcircuit Port	Part	Pin Names	Model	Model Type
ddr2_controller	ddr2_controller	freescaple	MDQ[[63:0]],MDQS[[8:0]],MDQS_B[[8:0]],MECC[[7:0]]	ddr2_io_full	I/O
ddr2_sdram	ddr2_sdram	ddr2_sdram	DQ[7:0],DQS,DQS#	DQFULL_533	I/O
ddr2_sdram1	ddr2_sdram1	ddr2_sdram	DQ[7:0],DQS,DQS#	DQFULL_533	I/O

Transfers:

Source(s)	Target(s)	From	To	Timed From	Transfer Model Overrides:
ddr2_controller	ddr2_controller	ddr2_contr...	ddr2_sdram	ddr2_contr...	ddr2_controller ddr2_io_half
ddr2_sdram	ddr2_sdram	ddr2_contr...	ddr2_sdra...	ddr2_contr...	ddr2_sdram DQHALF_800
ddr2_sdram1	ddr2_sdram1	ddr2_sdra...	ddr2_contr...	ddr2_sdra...	ddr2_sdram1 DQHALF_ODT75_...

Stimulus Setup in QSI

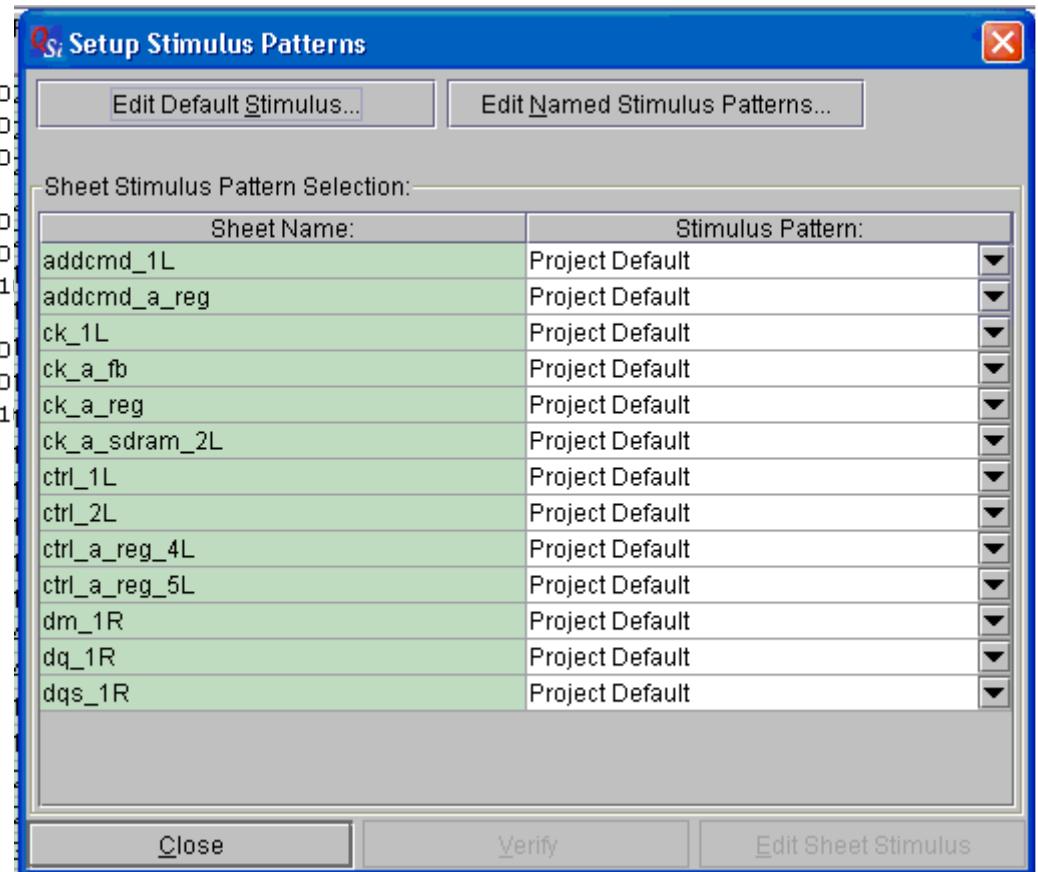
```
rise_time          100pS          Tj
character_time     100pS          Uj

*data              0110010101
* PRBS

data               000001011001000111110100110
data_victim        010101010101010101010101010
data_aggressor     000001011001000111110100110

clock              010101010101010101010101010
clock_victim       010101010101010101010101010
clock_aggressor    10101010101010101010101010101

strobe             010101010101010101010101010
strobe_victim      010101010101010101010101010
strobe_aggressor   10101010101010101010101010101
```



Waveform and Timing Report

	A	B	C	D	E	F	G	H	I	J	K	L	M	N
1	Setup Margin (ns)	Hold Margin (ns)	Rmin Etch Delay (ns)	Rmax Etch Delay (ns)	Fmin Etch Delay (ns)	Fmax Etch Delay (ns)	Transfer Net							
2	No AC specs	No AC specs	1.072	1.373	1.072	1.373	PRE_PLL_CLK							
3	No AC specs	No AC specs	0.403	0.617	0.403	0.613	PLL_SDRAM_CLK							
4	No AC specs	No AC specs	0.358	0.627	0.36	0.632	pll_reg_clk							
5	No AC specs	No AC specs	0.38	0.552	0.381	0.55	PLL_FDBK							
6	0.037	0.784	1.331	1.71	1.331	1.71	DQS_ECC_2R_2Slot							
7	0.153	0.585	1.206	1.616	1.205	1.614	DQS_2R_2Slot							
8	0.828	1.01	1.037	1.511	1.072	1.412	Pre_reg_cmd_slot1							
9	0.807	1.03	1.153	1.675	1.189	1.575	Pre_reg_cmd_slot2							
10	0.375	1.127	1.154	1.907	1.195	1.748	Pre_reg_CS							
11	0.617	1.006	1.033	1.865	1.067	1.744	Pre_reg_addcmd							
12	0.344	0.232	1.132	1.795	1.143	1.741	DQ_2R_2Slot							
13	0.395	0.305	1.293	1.662	1.294	1.603	DM_2R_2Slot							
14	1.223	1.411	0.827	1.244	0.771	1.312	Post_reg_addcmd_LB							
15	1.169	1.255	0.756	1.34	0.623	1.376	Post_reg_addcmd_RB							
16	1.442	1.228	0.701	1.091	0.615	1.08	Post_Reg_CTRL_4L							
17	0.875	1.356	0.819	1.592	0.733	1.656	Post_Reg_CTRL_5L							
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◀ ▶ 🔍 Waveform Quality / Waveform Overshoot / Eye Rollups / Eye Details / Waveform Margin By Tnet / Waveform Margin By Variation / Model Overview / Timing An:

Ready NUM

Summary

- Definition of HSD
- Static Timing Analysis for DDR
- Pre-route simulations (Scan the design space)
- Routing Rules development for CAD
- Full post route simulations
- Summary



References

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- Micron DDR2 Datasheet
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- SiSoft-Micron DDR2 Paper
<http://www.sisoft.com/papers.asp>

■ **Presentation Abstract:** PCB level SI tools and strategy

I will discuss the current tools and strategy my team uses use for PCB level high speed design. We can follow the design flow from the pre route simulation/ rule development, to the full post route verification of the design. Specifically we will examine use of the SiSoft tool for control of the Spice simulations and timing of the design for a DDR2 implementation.

Author Biography:

Stephen Searce is currently is working as the manager of the High Speed Design team at Cisco System Inc, and has worked in HSD team as a signal integrity engineer for 4 years at Cisco. Before joining the central HSD team, Stephen worked for the Cisco ATG as an EMC/Safety/NEBS designer. Prior to working at Cisco, Stephen worked for NASA LaRC as a research engineer in the Electromagnetics research branch HIRF team. His research interests include power integrity and signal integrity full channel design (Die to Die). Stephen has 3 US patents and 2 pending patents. He received his BS and MSEE from Old Dominion University, Norfolk VA.

Sincerely,

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