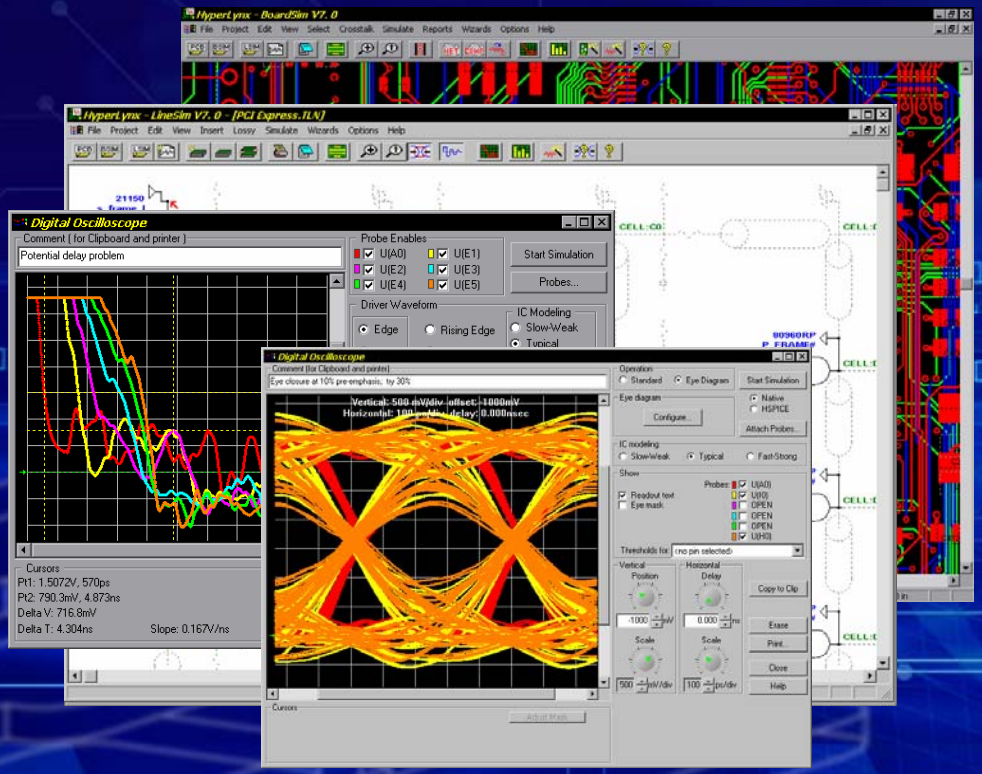
Mentor Graphics

DDR Memory So Easy, A Caveman Can Do It



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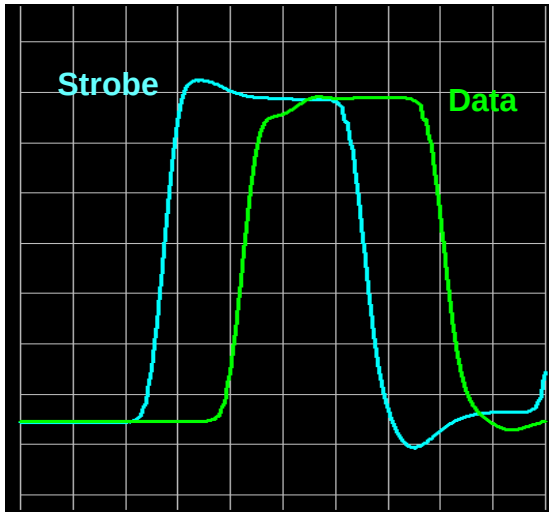
Mentor Graphics®

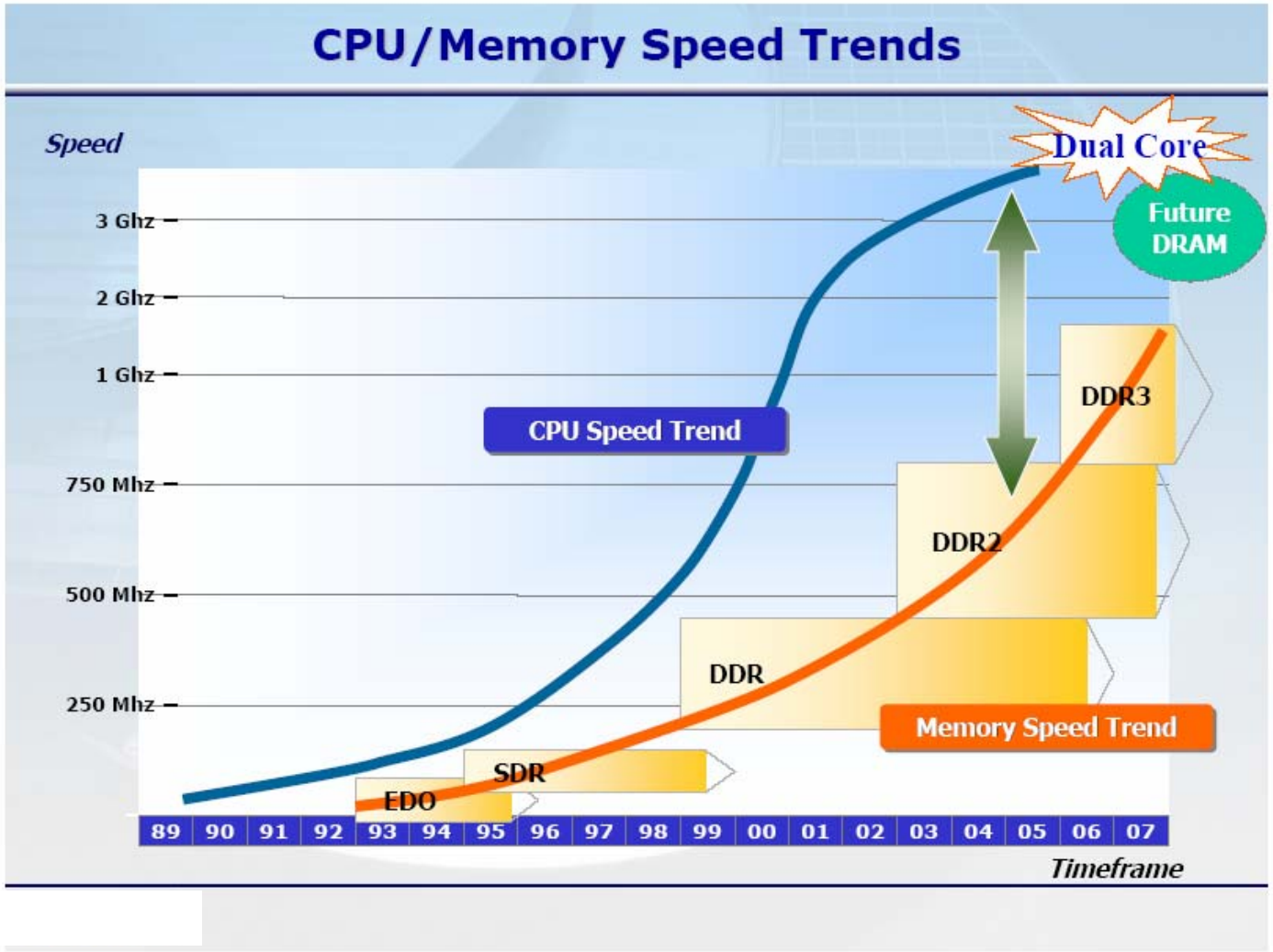
Agenda

DDR Memory design



1. **DDR/DDR2 Technology Overview**
2. **DDR/DDR2 Challenges and Layout Guidelines**
3. **Introduction to DDR3**
4. **Wrap up**

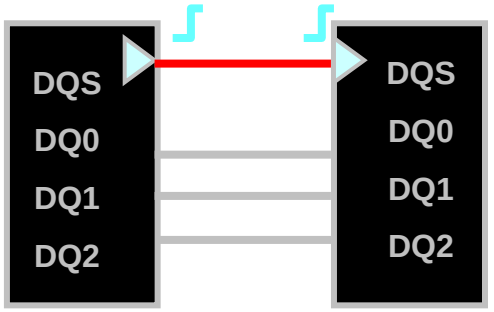
Memory Trends

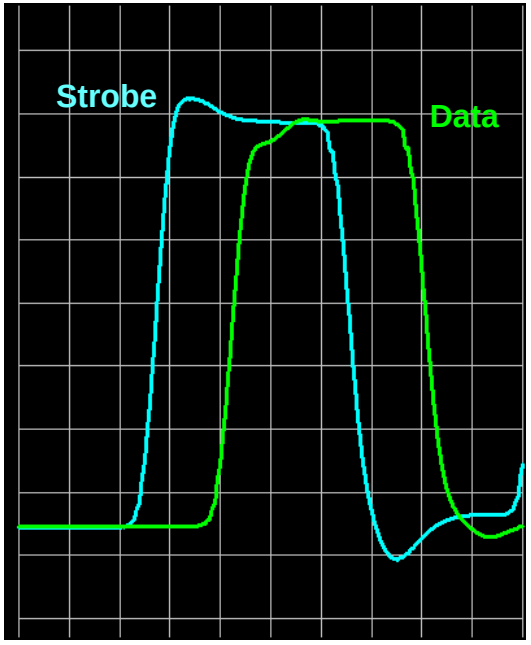


*Courtesy of Hynix Semiconductor

DDR Overview

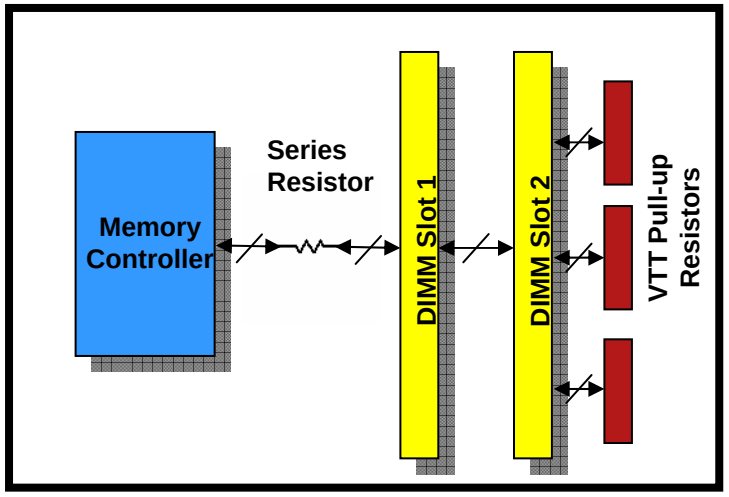
- **Double Data Rate (DDR) Memory**
  - Data is "clocked" in on both the rising and falling edge of the synchronous strobe signal
- **Source-synchronous interface**
  - Clock (Strobe) is routed along the same path as the data
  - Data/Strobe signals are bi-directional
  - Each data group has a corresponding strobe to minimize skew (data groups are 4, 8, or 16 bits wide) and optimize timing

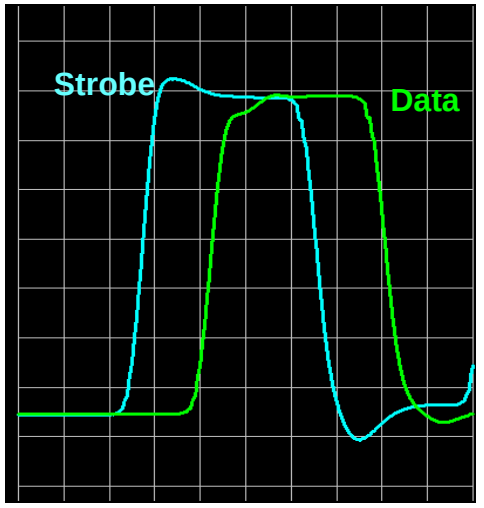




DDR Technology

- **DDR Operating Speeds**
  - **DDR200 (100 MHz clock)**
  - **DDR266 (133 MHz clock)**
  - **DDR333 (166.67 MHz clock)**
  - **DDR400 (200 MHz clock)**





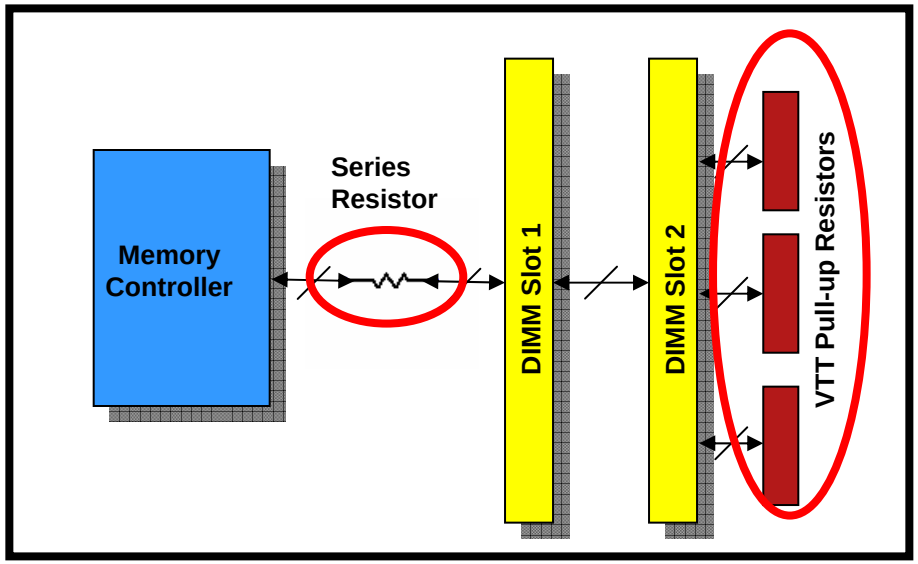
DDR Bandwidth

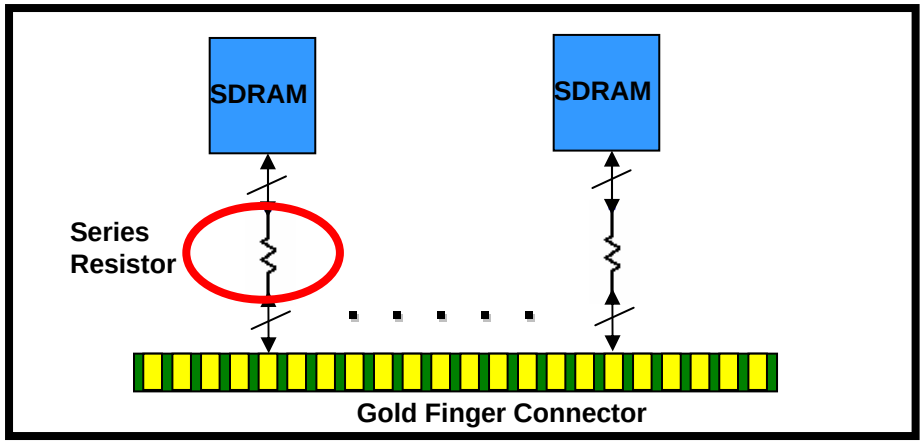
- **Improved bandwidth over Single Data Rate (SDR) memory**
  - **Same clock speed gives 2X the bandwidth**

Memory Bandwidth (Single Channel)					
SDR - SDRAM		DDR - SDRAM			
PC100	PC133	DDR200	DDR266	DDR333	DDR400
800 MB/s	1.1 GB/s	1.6 GB/s	2.1 GB/s	2.7 GB/s	3.2 GB/s

DDR Termination

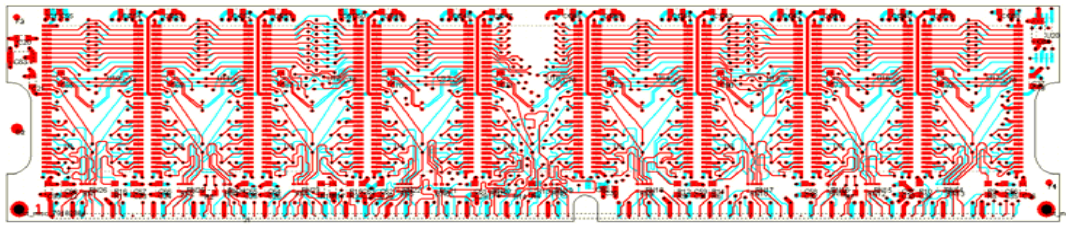
- **Termination**
  - **Requires series termination**
    - **Series terminator on DIMMs**
    - **Series terminator on your PCB**
  - **Pull-up termation to Vtt**





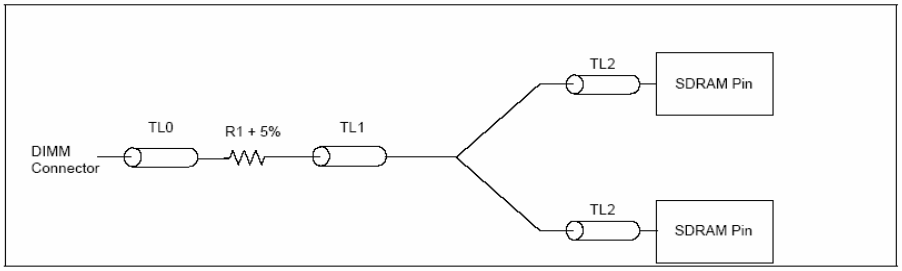
DDR DIMM Technology

- **DIMMS come in many configurations**
  - **x4, x8, x16 SDRAM devices**
  - **1 or 2 Physical Memory Banks**
  - **Registered or Unbuffered Address/CMD signals**
  - **Non-parity (x64 bits) or ECC (x72 bits)**
- **Tend to have the same routing even if from different vendors**
  - **Many manufacturers share DIMM layout data**

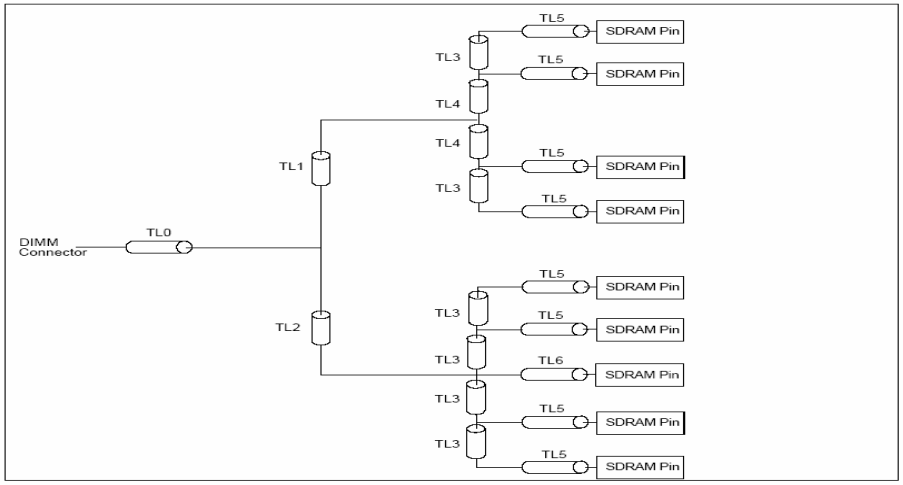


DDR Unbuffered DIMMs

- **Address signals - Unbuffered**
  - **Data/Strobe**

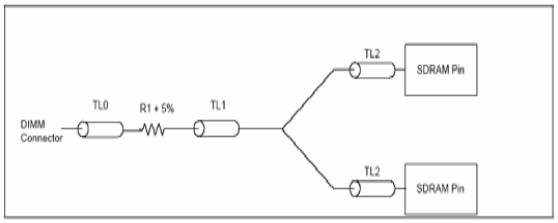


  - **Address/Control**

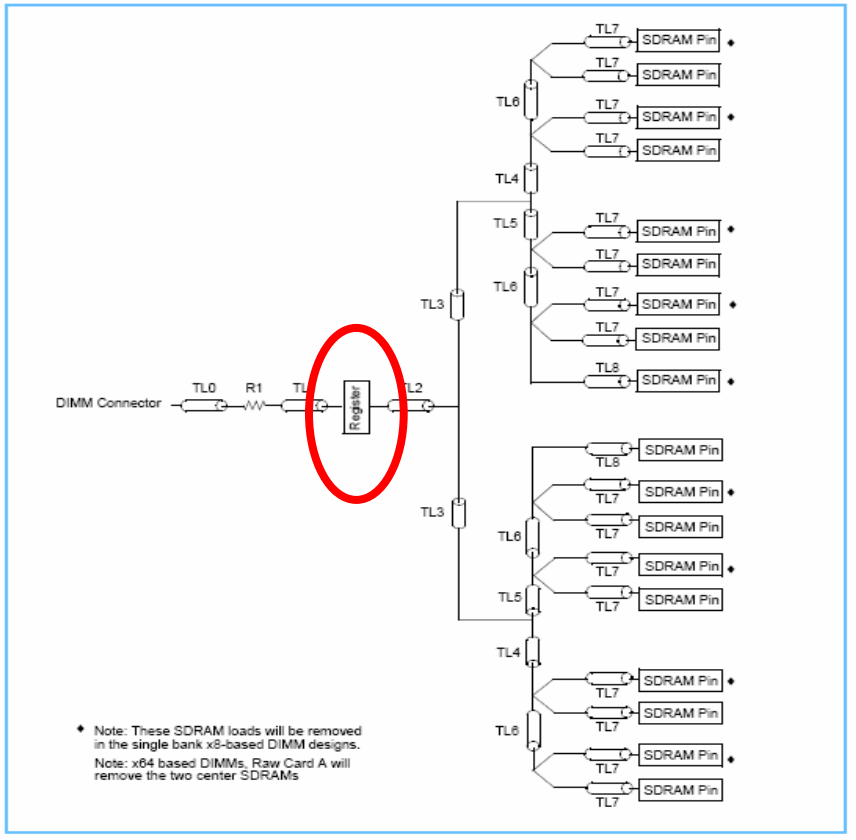


DDR Registered DIMMs

- **Address signals - Registered**
  - **Data/Strobe**

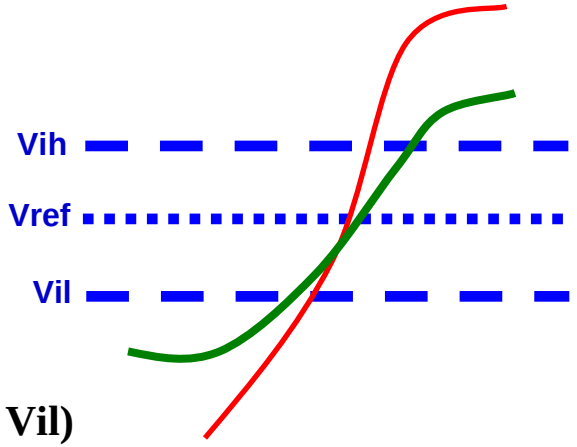


  - **Address/Control**



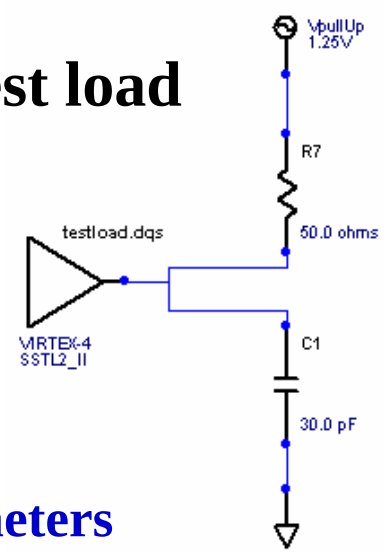
DDR Electrical Characteristics

- DDR uses SSTL_2 buffer technology
  - 2.5V technology
  - Class I drivers for point to point connection – Half drive strength
  - Class II drivers for multi-drop connection – Full drive strength
- Some important voltages to remember
  - Vref = 1.25V
    - Used for setting up timing thresholds (Vih and Vil)
    - Must be kept stable
  - Vih = 1.56V Nominal
    - Vref + 0.31 - Logic high threshold
  - Vil = 0.97V Nominal
    - Vref – 0.31 - Logic low threshold



DDR Timing Characteristics

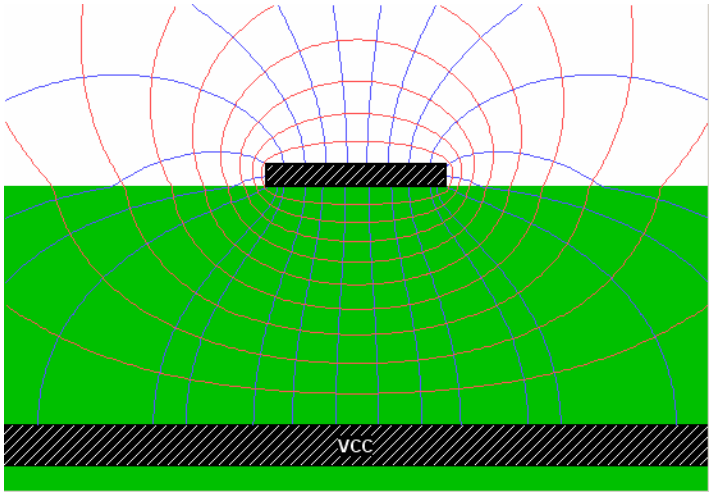
- Flight time measurements into a JEDEC test load
  - 30 pF to Ground
  - 50 ohm pull-up to Vref (nominally 1.25V)
- Some important timing parameters needed for timing equations



- **Setup time parameters**
  - Tck = Clock cycle time
  - Tipw = DQ and DM pulse width
  - Tdipw = Address Control pulse width
  - Tdqsh/l = DQS high/low pulse width
  - Tds = DQ and DM setup time to DQS
  - Tdqsq = DQS setup skew from associated DQ/DM signals
  - Tdss = Falling edge DQS to CLK setup time
  - Tis = Address/CMD setup time to CLK
- **Hold time parameters**
  - Tck = Clock cycle time
  - Tipw = DQ and DM pulse width
  - Tdipw = Address Control pulse width
  - Tdqsh/l = DQS high/low pulse width
  - Tdh = DQ and DM hold time to DQS
  - Tdqhq = DQS hold skew between associated DQ/DM signals
  - Tdsh = Falling edge DQS hold time from CLK
  - Tih = Address/CMD hold time to CLK

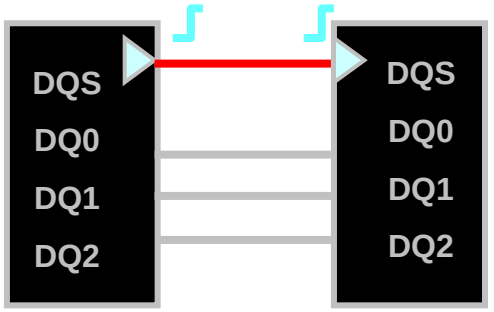
DDR Impedance Characteristics

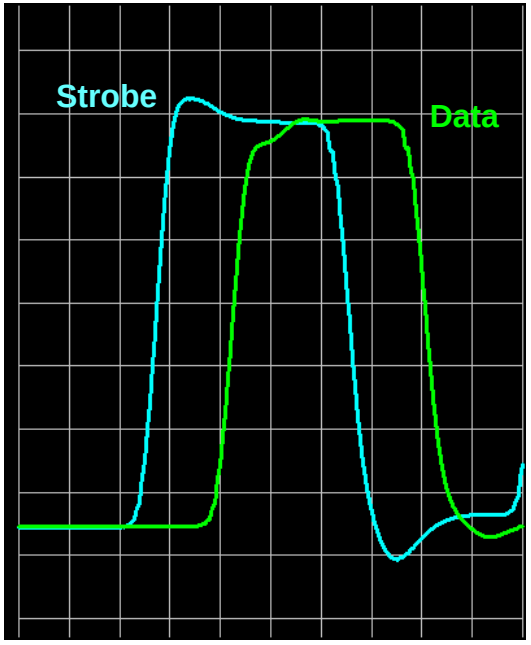
- **Recommended impedance of 60 ohms**
  - **Best to simulate with different impedance values to determine the best solution**



DDR2 Technology

- **DDR2 Operating Speeds**
  - **DDR2-400 (200 MHz clock)**
  - **DDR2-533 (266 MHz clock)**
  - **DDR2-667 (333 MHz clock)**
  - **DDR2-800 (400 MHz clock)**
- **Source-Synchronous interface like original DDR**





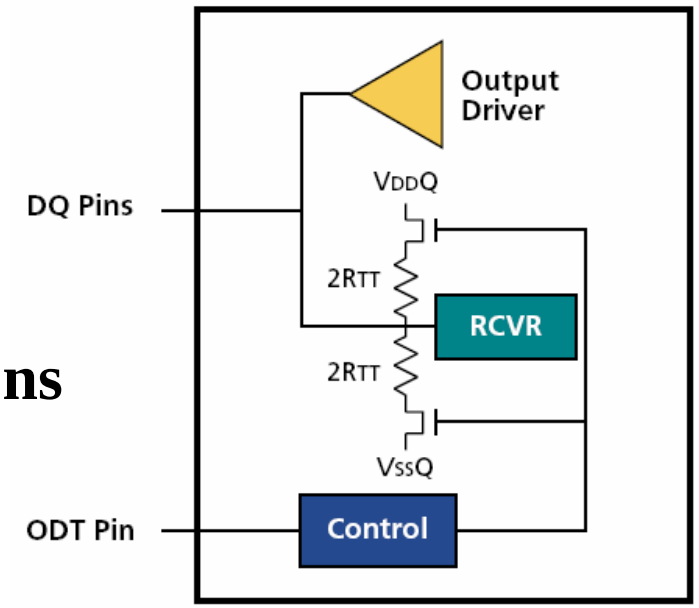
DDR2 Bandwidth

- **Not necessarily improved bandwidth over DDR**
  - **Original DDR2 has higher latency than DDR reducing effective bandwidth.**
  - **New lower latency DDR2 memory modules are improving this gap**

Memory Bandwidth (Single Channel)					
DDR		DDR2			
DDR333	DDR400	DDR2-400	DDR2-533	DDR2-667	DDR2-800
2.7 GB/s	3.2 GB/s	3.2 GB/s	4.266 GB/s	5.33 GB/s	6.4 GB/s

DDR2 On Die Termination

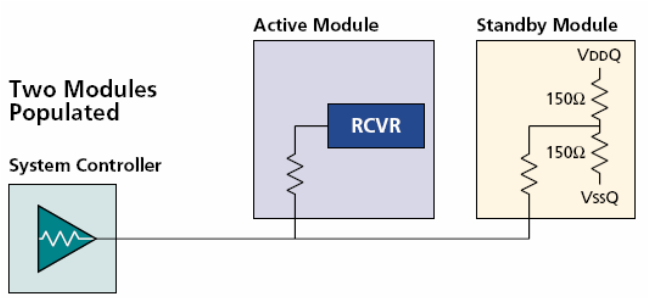
- **ODT – On Die Termination**
  - **Built into the controller and SDRAM**
  - **Offers multiple termination values for different configurations**
    - **50 Ohm, 75 Ohm, 150 Ohm**
  - **Turns on or off depending on Read/Write cycle**

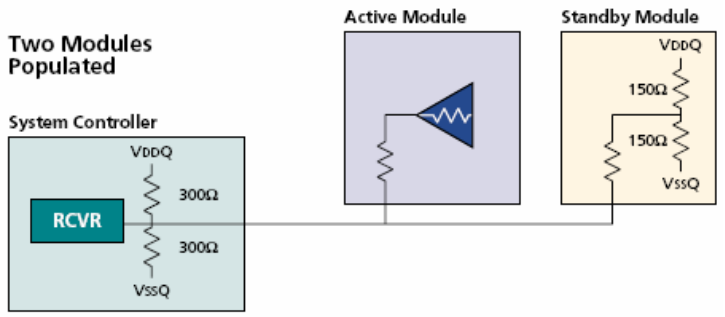


* Courtesy of Micron

DDR2 On Die Termination

- **How ODT works – Example of a 2 module system**
  - **Write operation**
    - **ODT off at Controller**
    - **DIMM receiving data has ODT of 150 Ohms**
    - **DIMM not receiving data has ODT of 75 Ohms**
  - **Read operation**
    - **ODT off at driving DIMM**
    - **ODT 150 Ohms at Controller**
    - **DIMM not driving has ODT of 75 Ohms**

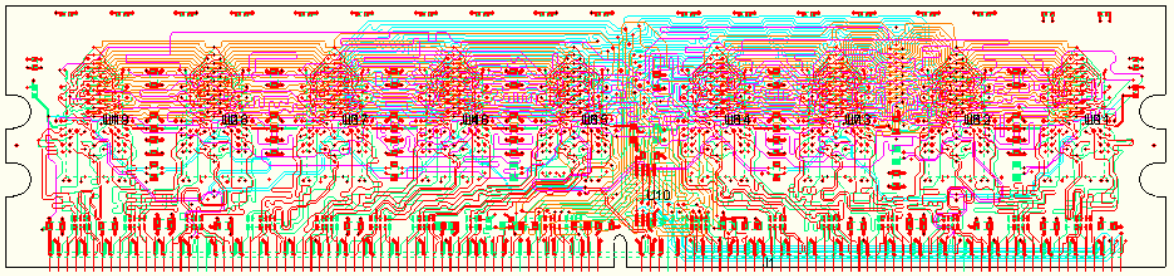




* Courtesy of Micron

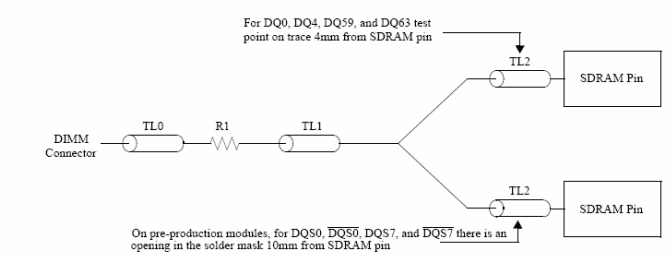
DDR2 DIMM Technology

- **Same as DDR, DIMMs come in many configurations**
  - **x4, x8, x16 SDRAM devices**
  - **1, 2 or 4 Rank (or Bank) DIMMs**
  - **Registered or Unbuffered Address/CMD signals**
  - **Non-ECC (x64 bits) or ECC (x72 bits)**
  - **Parity or no Parity for Address signals**
  - **Stacked or un-Stacked components**
- **DIMM layout is controlled by JEDEC**
  - **Many manufacturers shared responsibility of creating the DIMM layout data**

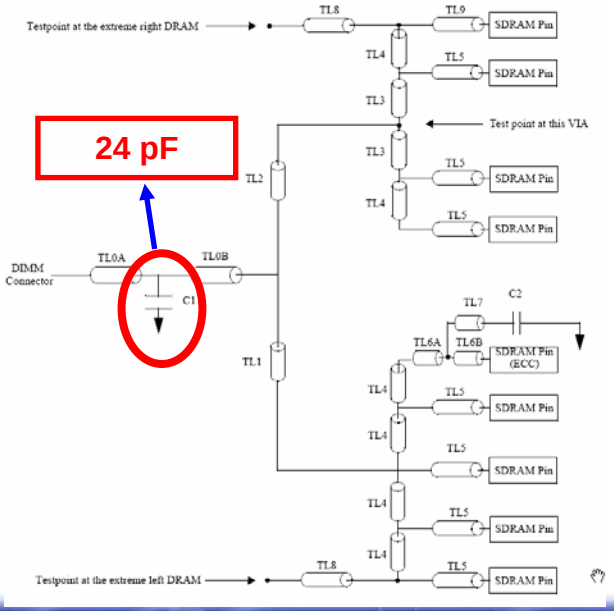


DDR2 Unbuffered DIMMs

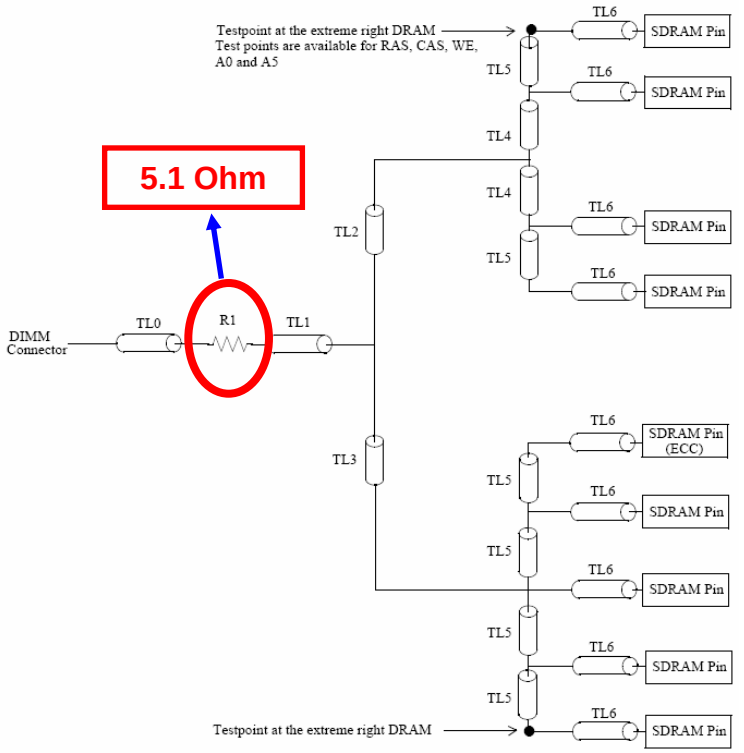
- Data/Strobe



- ODT control

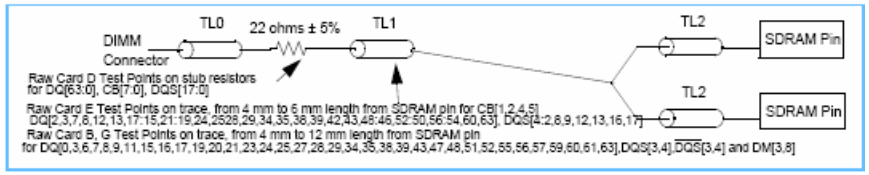


- Address/Control

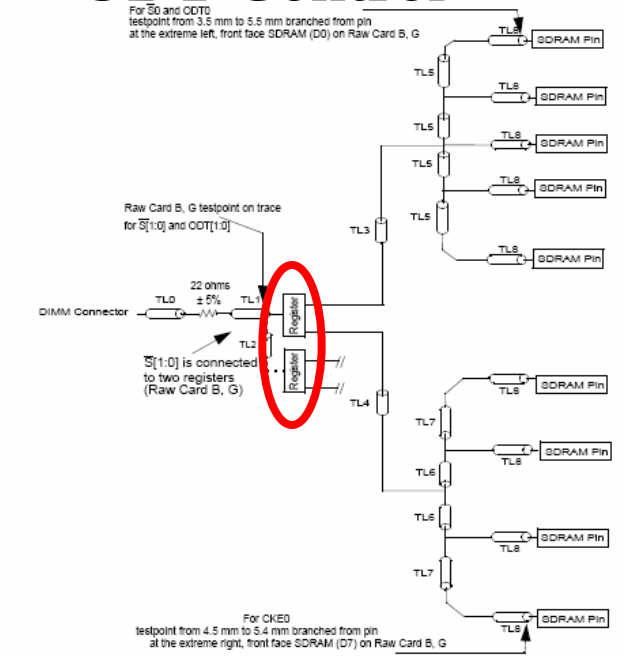


DDR2 Registered DIMMs

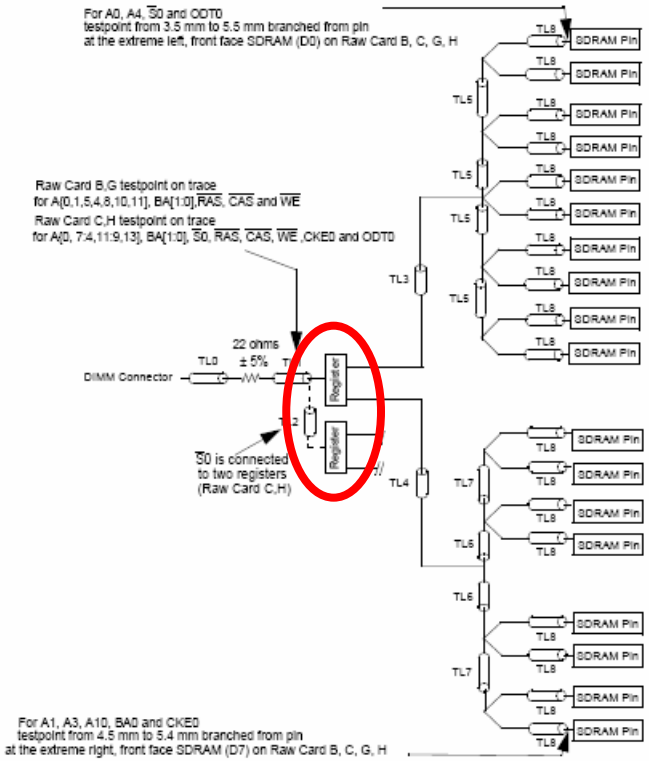
– **Data/Strobe**



– **ODT Control**

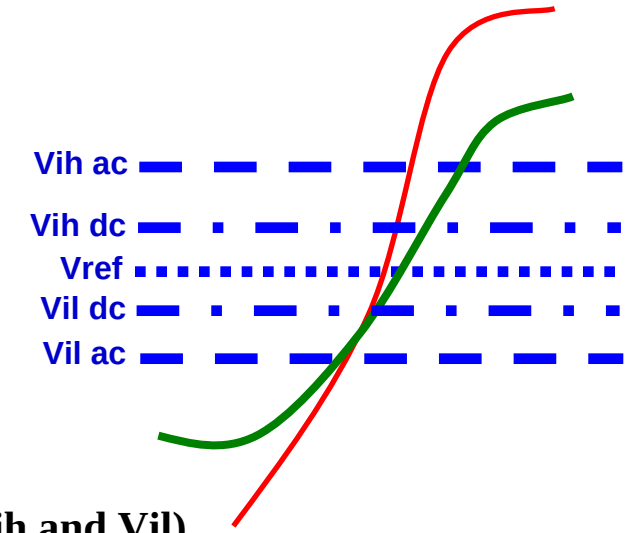


– **Address/Control**



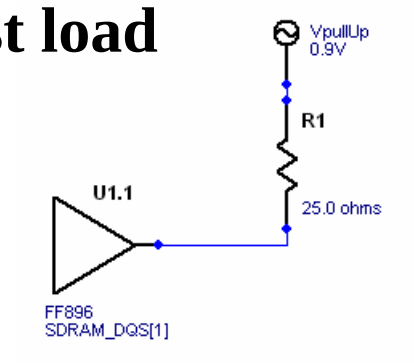
DDR2 Electrical Characteristics

- DDR2 uses SSTL18 buffer technology
  - 1.8V technology
  - Class I drivers for point to point connection – Half drive strength
  - Class II drivers for multi-drop connection – Full drive strength
- Some important voltages to remember
  - Vref = 900 mV
    - Used for setting up switching thresholds (Vih and Vil)
  - Vih/Vil AC Thresholds
    - = Vref +/- 250 mV for DDR2-400 & 533
    - = Vref +/- 200 mV for DDR2-667 & 800
  - Vih/Vil DC Thresholds
    - =Vref +/- 125 mV for all DDR2



DDR2 Timing Characteristics

- Flight time measurements into a JEDEC test load
  - 25 ohm pull-up to Vtt (nominally 900 mV)
- Some important timing parameters needed for timing equations



- **Setup time parameters**
  - Tck = Clock cycle time
  - Tipw = DQ and DM pulse width
  - Tdipw = Address Control pulse width
  - Tdqsh/l = DQS high/low pulse width
  - Tds = DQ and DM setup time to DQS
  - Tdqsq = DQS setup skew from associated DQ/DM signals
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- **Hold time parameters**
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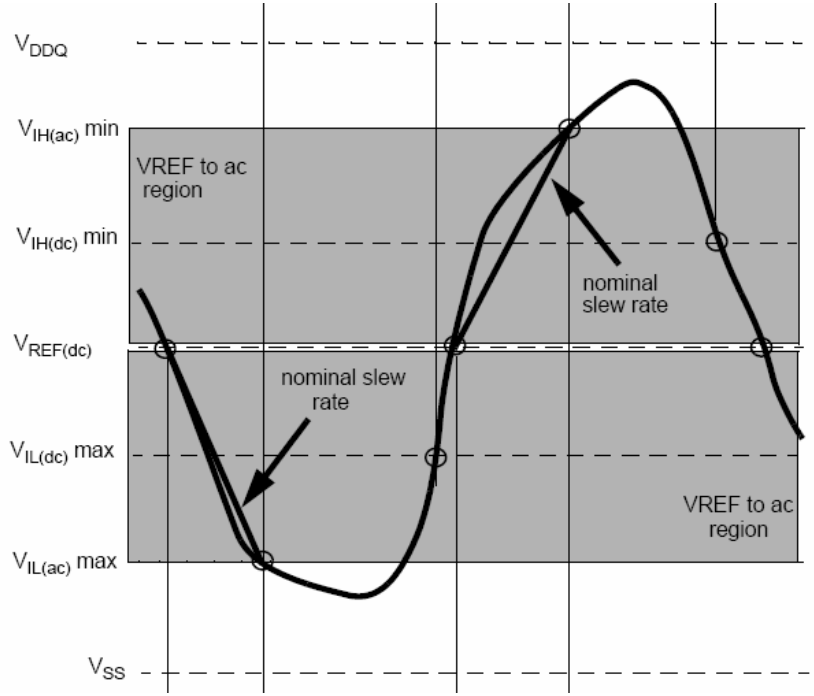
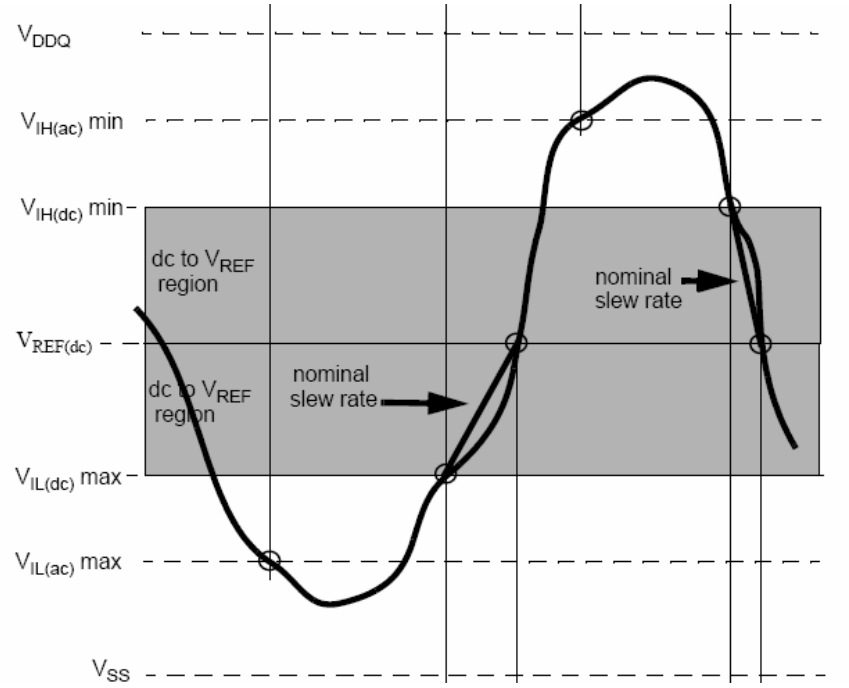
  - Tdqhq = DQS hold skew between associated DQ/DM signals
  - Tdsh = Falling edge DQS hold time from CLK
  - Tih = Address/CMD hold time to CLK

DDR2 Timing Characteristics

- **Signal derating required to meet setup and hold times**
  - **Find nominal slew rate**
    - **Setup**

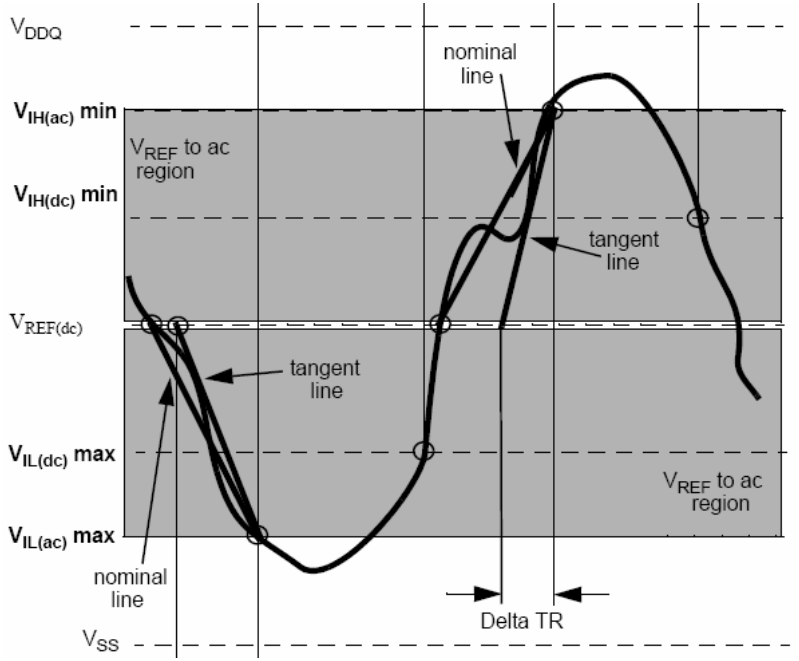


    - **Hold**

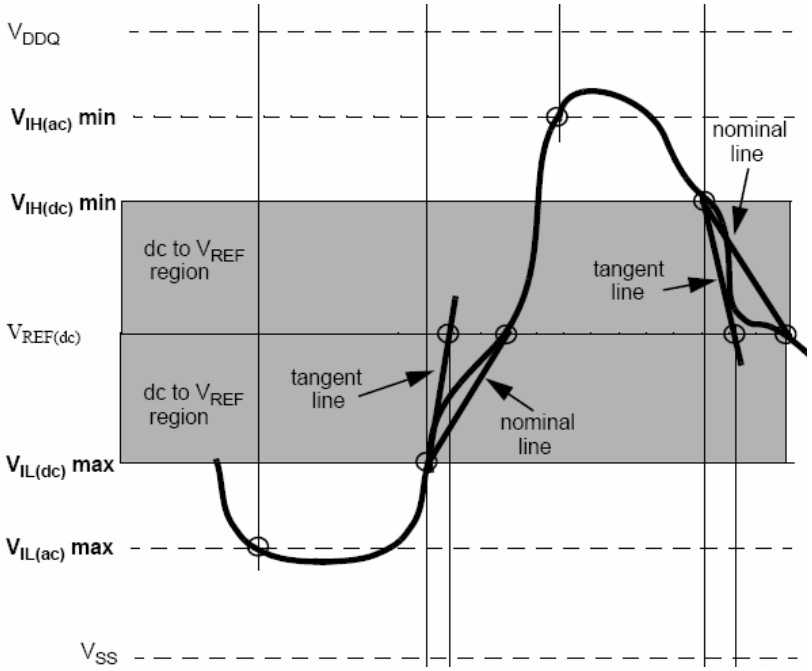


DDR2 Timing Characteristics

- **Setup**
  - If any of the signal falls to the right of the nominal slew rate in the switching region, signal must be derated

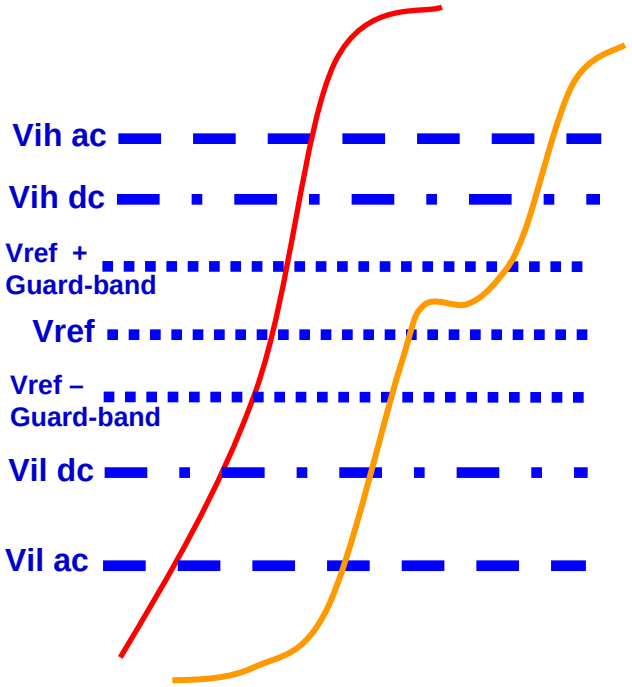


- **Hold**
  - If any of the signal falls to the left of the nominal slew rate in the switching region, signal must be derated



DDR2 Timing Characteristics

- **Setup slew rate measurement**
  - **Rising Edge**
    - **Last crossing of Vref + DC Guard-band to first crossing of Vih-ac**
  - **Falling Edge**
    - **Last crossing of Vref – DC Guard-band to first crossing of Vil-ac**
- **Hold slew rate measurement**
  - **Rising Edge**
    - **First crossing of Vil-dc to the first crossing of Vref – AC Guard-band**
  - **Falling Edge**
    - **First crossing of Vih-dc to the first crossing of Vref + AC Guard-band**



DDR2 Timing Characteristics

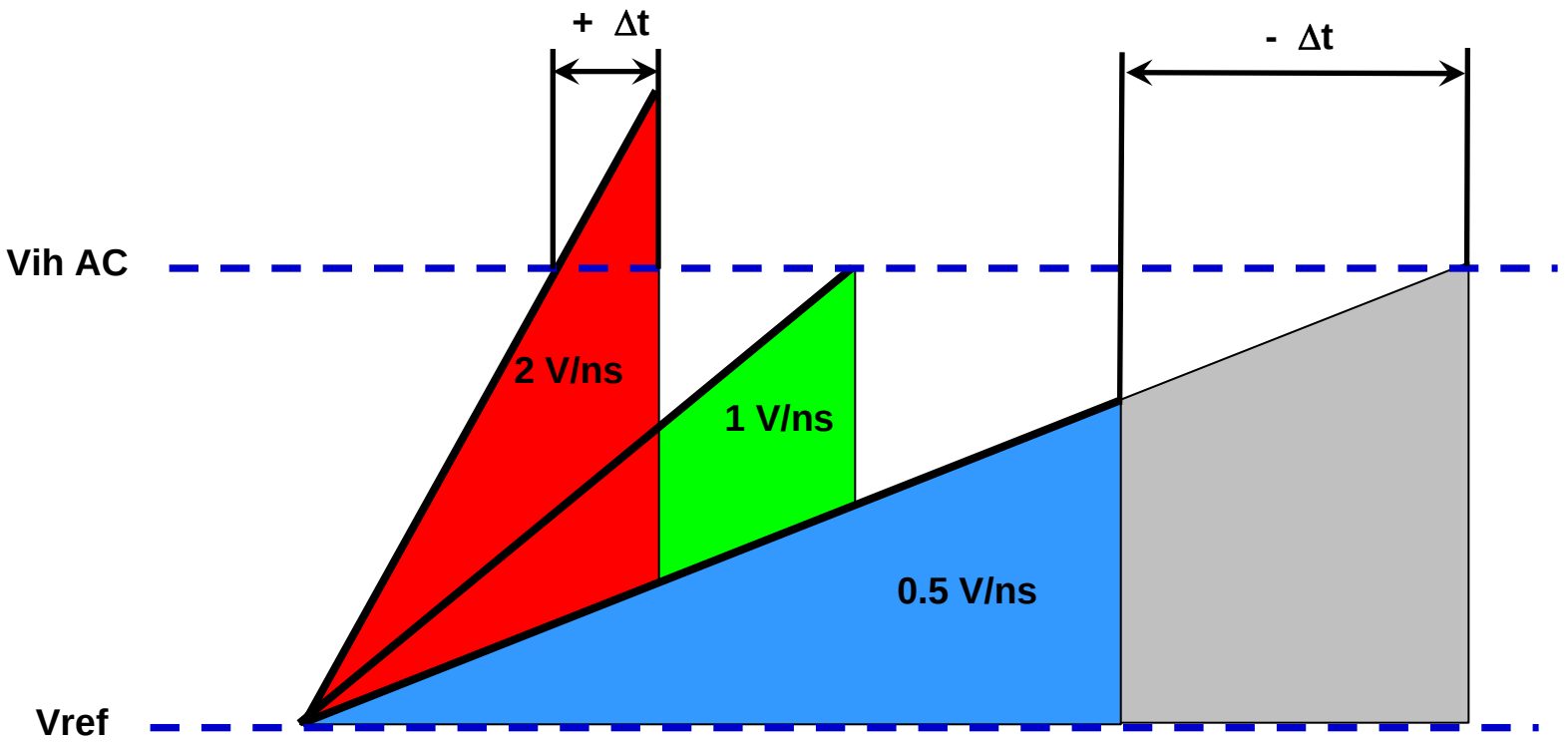
- **Derate or Prorate setup and hold times based on slew rate information**

Table 45 — Derating values for DDR2-400, DDR2-533.

tIS, tIH Derating Values for DDR2-400, DDR2-533									
		CK,CK Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Com-mand/Ad-dress Slew rate (V/ns)	4.0	+187	+94	+217	+124	+247	+154	ps	1
	3.5	+179	+89	+209	+119	+239	+149	ps	1
	3.0	+167	+83	+197	+113	+227	+143	ps	1
	2.5	+150	+75	+180	+105	+210	+135	ps	1
	2.0	+125	+45	+155	+75	+185	+105	ps	1
	1.5	+83	+21	+113	+51	+143	+81	ps	1
	1.0	0	0	+30	+30	+60	60	ps	1
	0.9	-11	-14	+19	+16	+49	+46	ps	1
	0.8	-25	-31	+5	-1	+35	+29	ps	1
	0.7	-43	-54	-13	-24	+17	+6	ps	1
	0.6	-67	-83	-37	-53	-7	-23	ps	1
	0.5	-110	-125	-80	-95	-50	-65	ps	1
	0.4	-175	-188	-145	-158	-115	-128	ps	1
	0.3	-285	-292	-255	-262	-225	-232	ps	1
	0.25	-350	-375	-320	-345	-290	-315	ps	1
	0.2	-525	-500	-495	-470	-465	-440	ps	1
	0.15	-800	-708	-770	-678	-740	-648	ps	1
	0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps	1

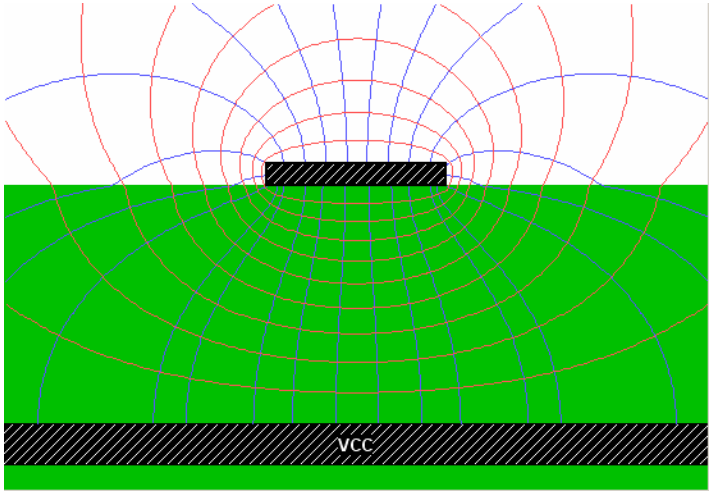
DDR2 Timing Characteristics

- **Why Derating?**
  - **Consider the area under the curve – Charge Model concept**



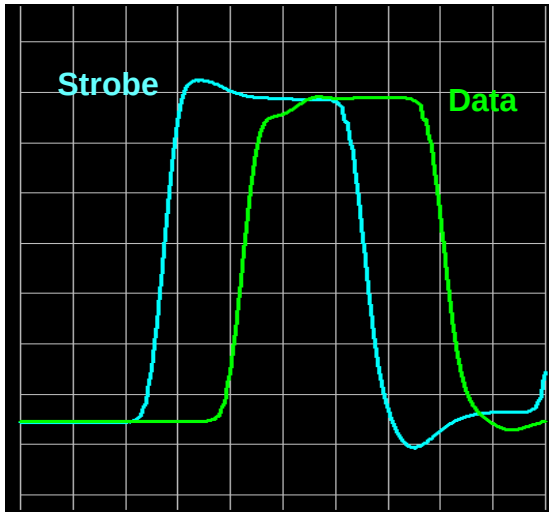
DDR2 Impedance Characteristics

- **Recommended impedance of 50 ohms**
  - **10 ohms lower than DDR**
  - **Simulate with different impedance values to determine the best solution**



Agenda

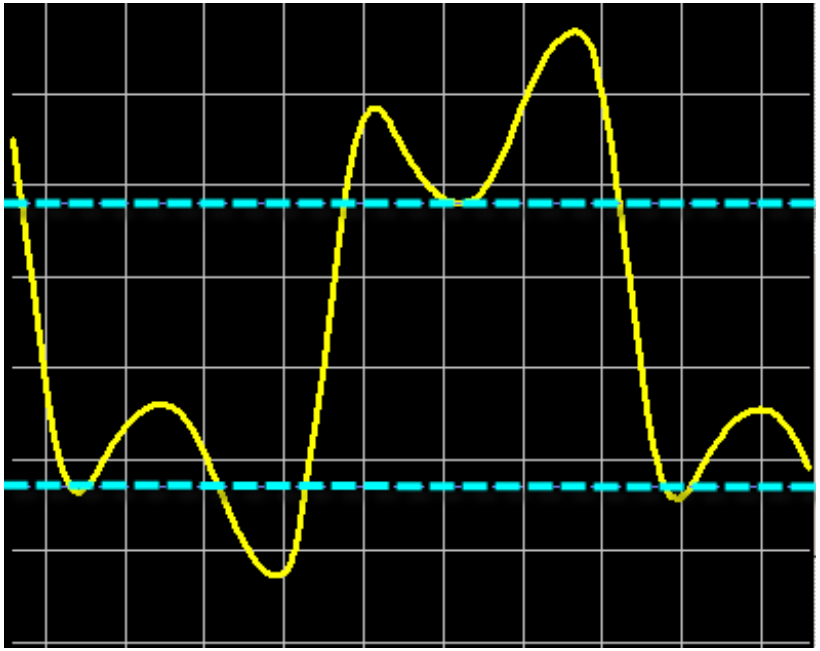
DDR Memory design

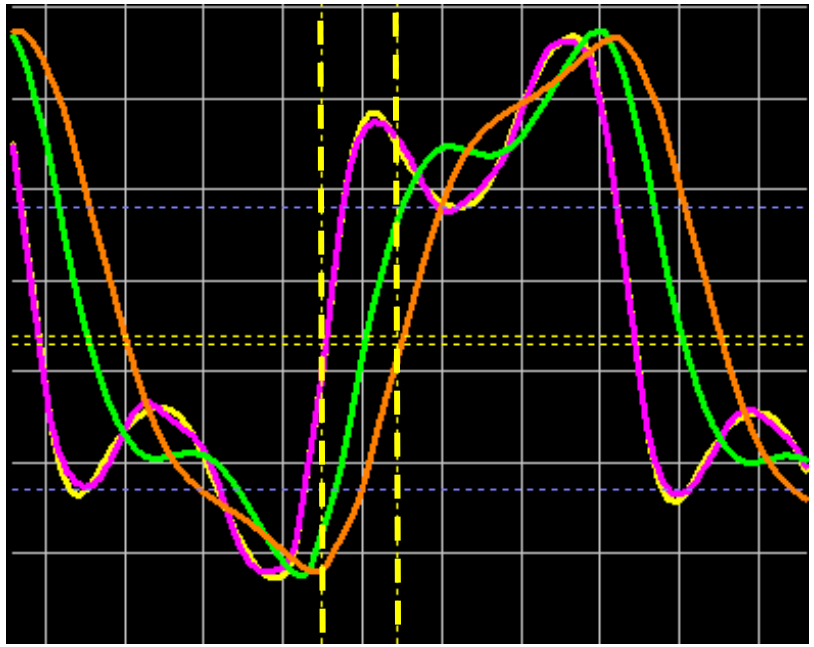


1. **DDR/DDR2 Technology Overview**
2. **DDR/DDR2 Challenges and Layout Guidelines**
3. **Introduction to DDR3**
4. **Wrap up**

DDR/DDR2 Design Challenges
Reflections and Skew

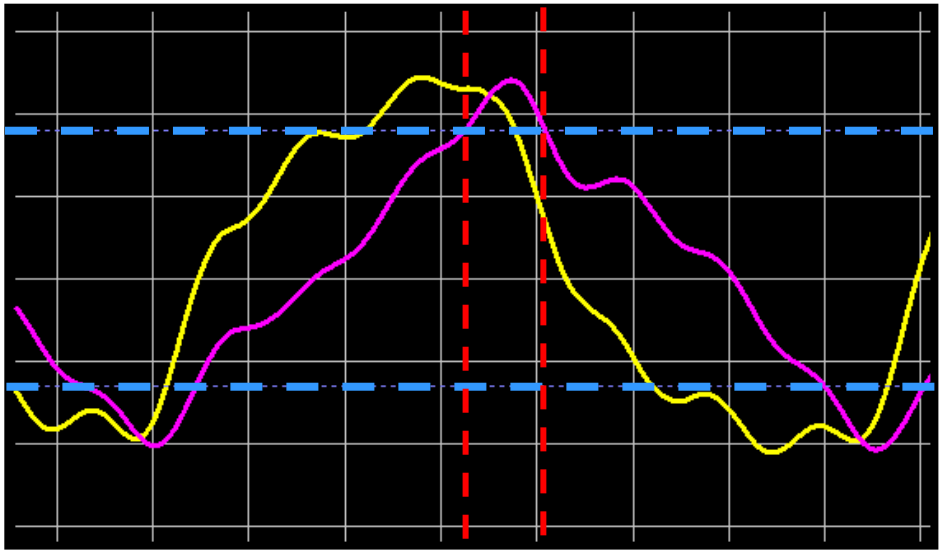
- Reflections seen on signal edges
- Skew between DQ bits consuming timing budget





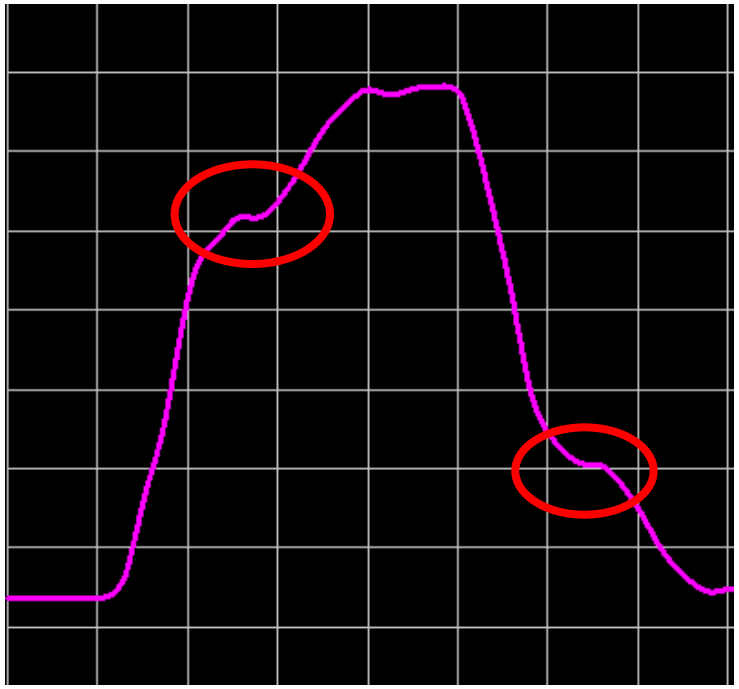
DDR/DDR2 Design Challenges
Address timing

- Very little timing budget for Address/Control signals under heavily loaded conditions



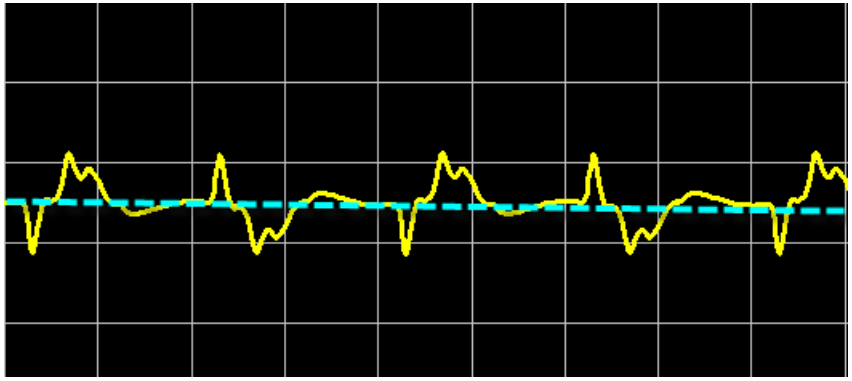
DDR/DDR2 Design Challenges
Crosstalk

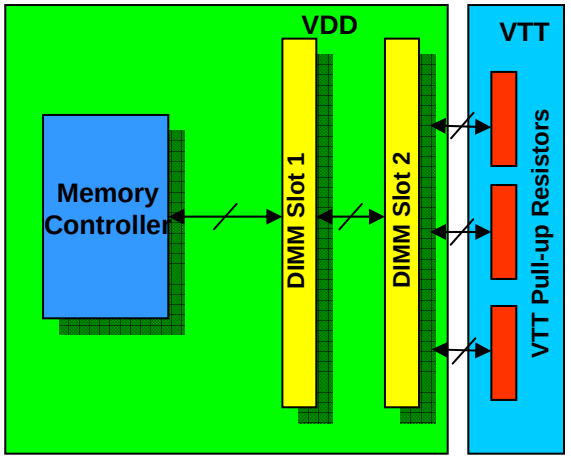
- **Crosstalk on Strobe Signals**
  - Often seen as “glitches” on the strobe edges
  - Can cause double clocking



DDR/DDR2 Design Challenges
Power Plane Stability

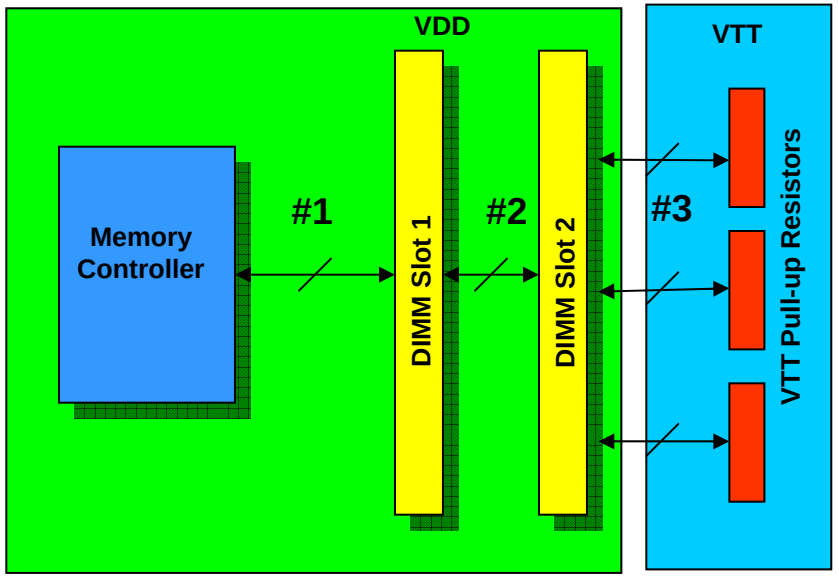
- **Vref and VDD Stability**
  - **SSO can cause fluctuations in Vref due to inadequate decoupling**
    - **Causes the Vref level to shift which changes the Vih and Vil switching thresholds**





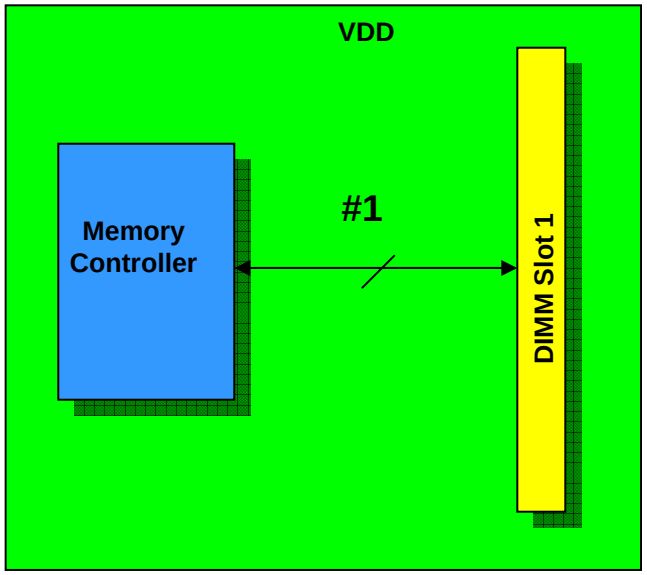
DDR Design Guidelines

- **What results are important**
  - **We need to constrain 4 critical lengths**
    1. **Net length from the controller to the 1st DIMM slot**
    2. **Net length between DIMM slots**
    3. **Net length from last slot to the Termination**
    4. **All DQS/DQ groups should be length matched to minimize skew within the group and across the channel**



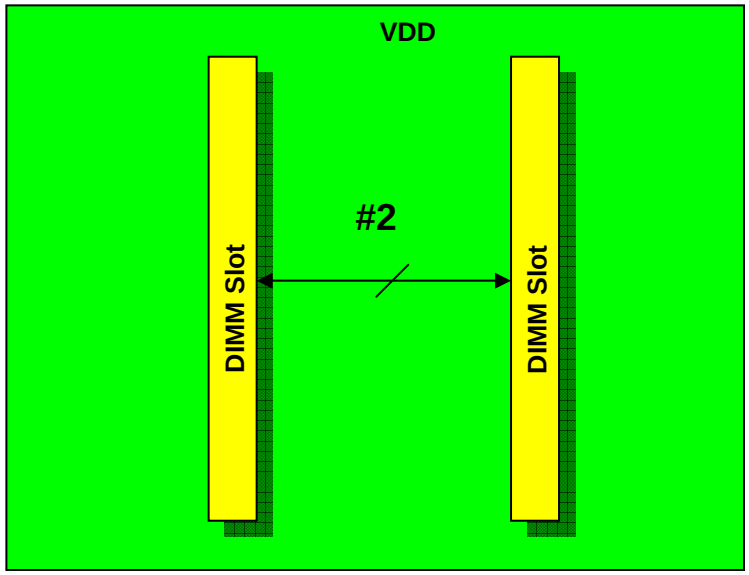
DDR Design Guidelines

- **What results are important**
  - **#1 This length is typically between 2” and 6” but dependant on the controller used and how many DIMMs are supported in a channel**
  - **Keep the series terminator as close as possible to the controller - typically within 1”**
    - **This length counts as part of the overall constraint for length #1**



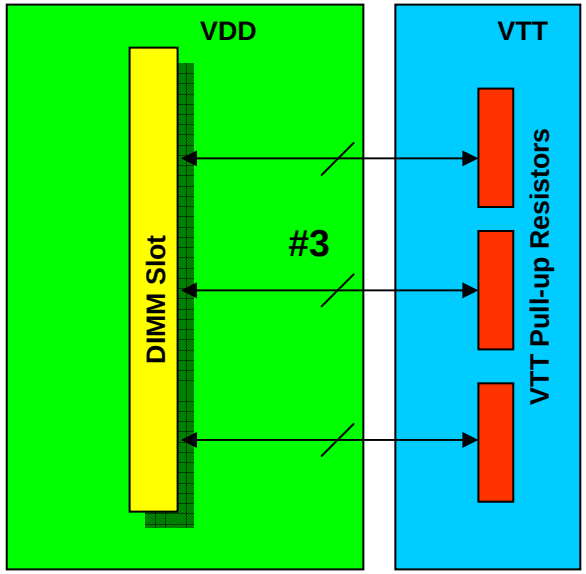
DDR Design Guidelines

- **What results are important**
  - **#2 This length is typically between 400 mils to 1.2”**
  - **Wider = Better airflow = Improved Thermals**
  - **But too wide can produce poor signal quality (SI)**



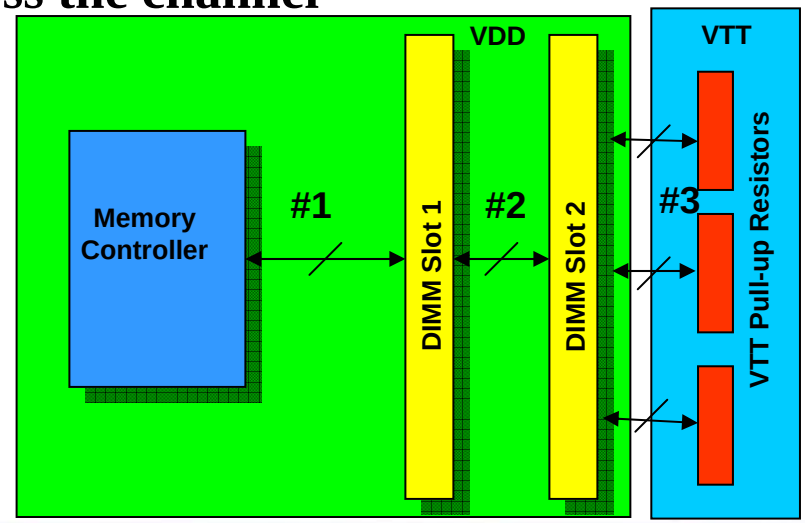
DDR Design Guidelines

- **What results are important**
  - **#3 This length does not have to be as tightly constrained as the other lengths since it only goes to a termination**
    - **No timing importance here**
  - **Typical constraint is from 500 mils to 2”**



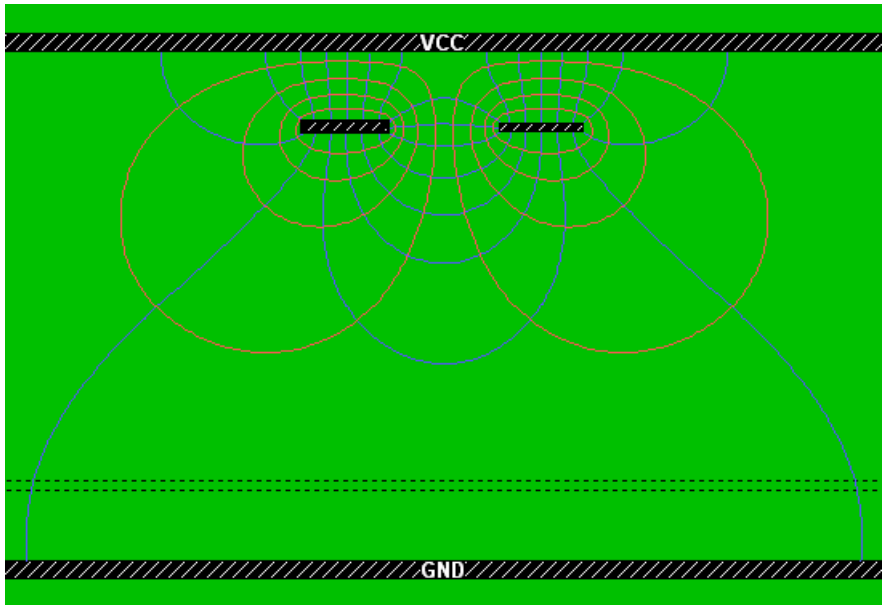
DDR Design Guidelines

- **What results are important**
  - #4 This constraint is very critical.
  - A data group (DQ) has an associated strobe (DQS);
  - This group should be length matched to each other with minimum skew
  - Typical constraints are about 50 mils within the group
    - Try to spread this out across the channel
    - +/- 25 mils for length #1
    - +/- 15 mils for length #2
    - +/- 15 mils for length #3
    - Helps to minimize skew between the DIMMs



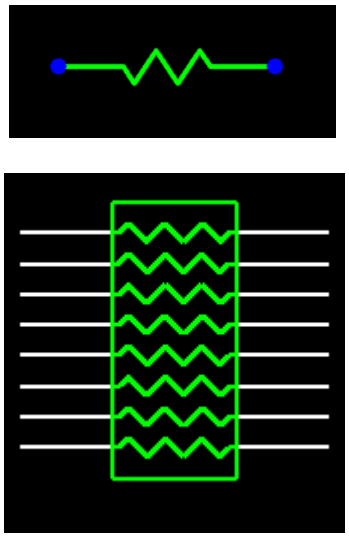
DDR Design Guidelines

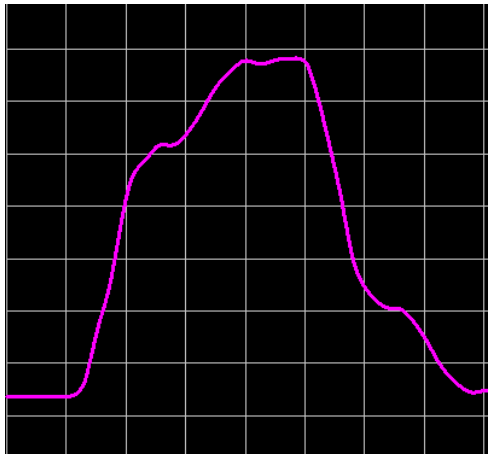
- **Spacing Recommendations**
  - Varies depending on stackup
  - Typically rules of thumb say 3H spacing
    - For a 6 mil dielectric this would be 18 mils
    - For signals coupled closely to reference planes, often 1.5H can be used



DDR Design Guidelines

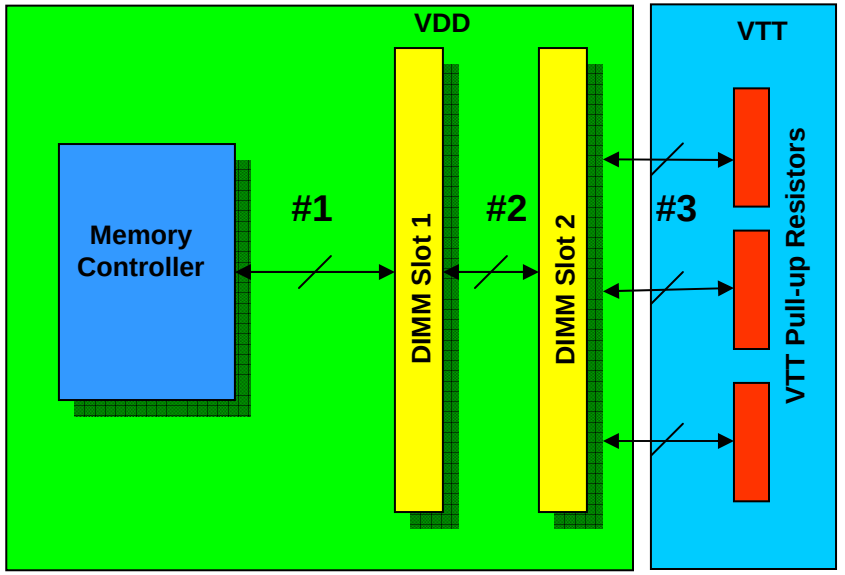
- **Terminations**
  - Use discrete components for DQS lines
  - R-packs typically have poor isolation
    - Causes Crosstalk problems on strobes





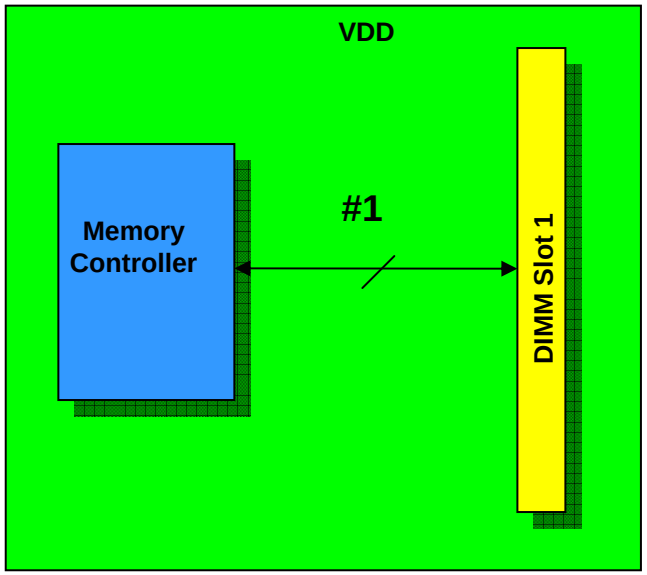
DDR2 Design Guidelines

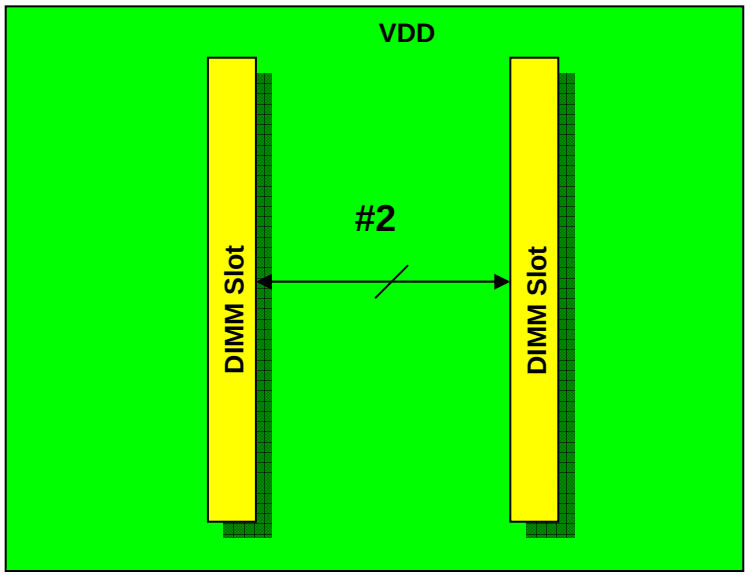
- **What results are important**
  - **We need to constrain 4 critical lengths**
    1. **Net length from the controller to the 1st DIMM slot**
    2. **Net length between DIMM slots**
    3. **Net length from last slot to the pull-up termination (only Address/Command)**
    4. **All DQS/DQ groups should be length matched to minimize skew within the group and across the channel**



DDR2 Design Guidelines

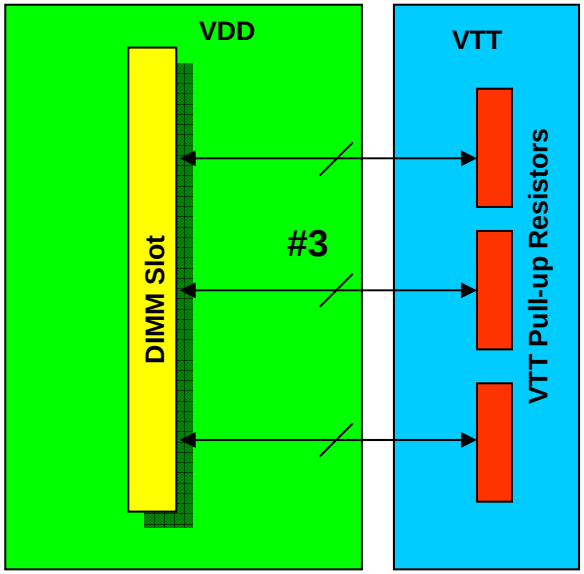
- **What results are important**
  - **#1 This length from the controller to the first DIMM is typically between 1.9” and 4.5”**
  - **#2 The length between the DIMMs is typically around 425 mils**





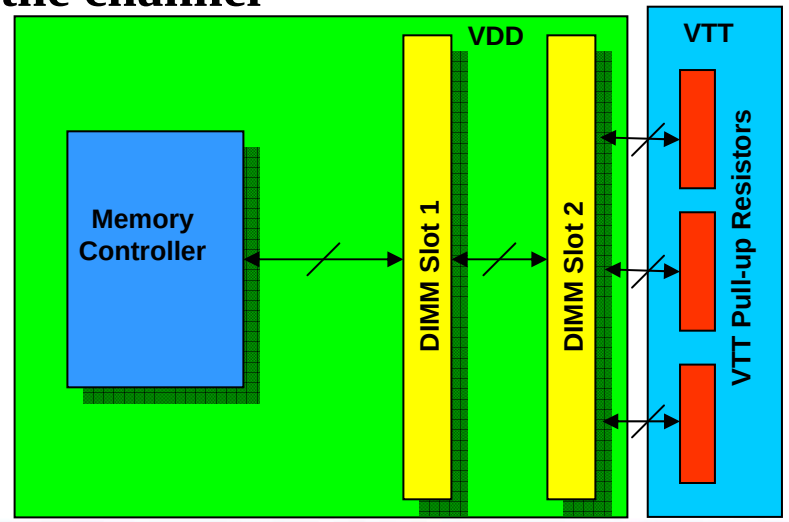
DDR2 Design Guidelines

- **What results are important**
  - **#3 The length from the last DIMM to the pull-up resistors is typically 200 mils to 550 mils**
    - **Only applies to the Address and Command nets – Data nets use ODT**
    - **No timing importance here**



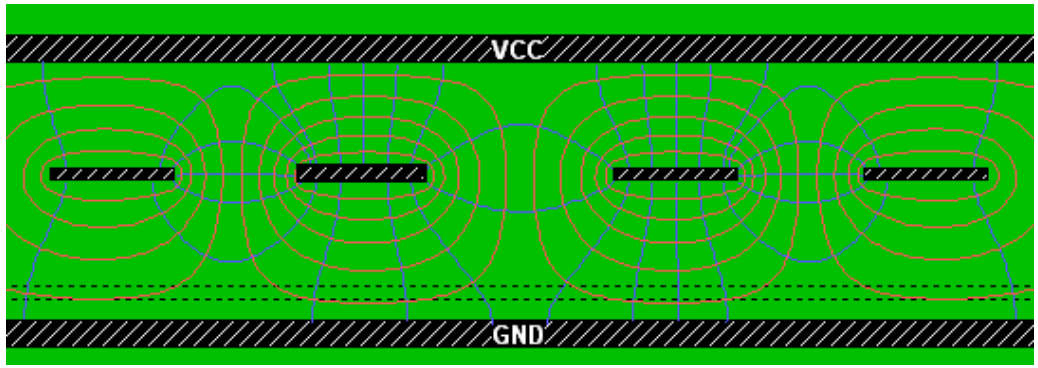
DDR2 Design Guidelines

- **What results are important**
  - #4 This constraint is very critical.
  - A data group (DQ) has an associated strobe (DQS);
  - This group should be length matched to each other with minimum skew
  - Typical constraints are about 50 mils within the group
    - Try to spread this out across the channel
    - +/- 30 mils for length #1
    - +/- 20 mils for length #2
    - Overall skew between byte lanes should be +/- 500 mils
    - Skew between address nets should be +/- 200 mils



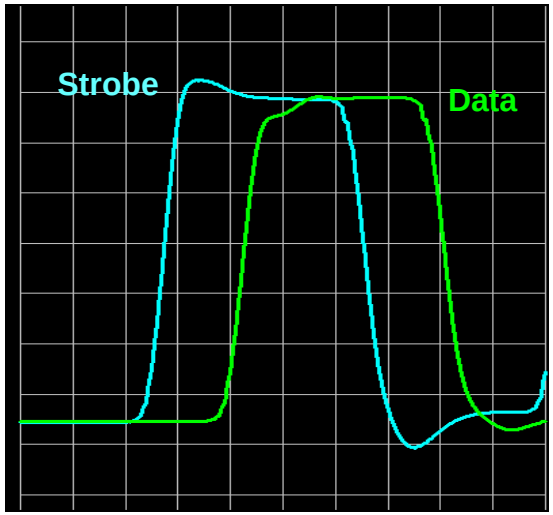
DDR2 Design Guidelines

- **Spacing Recommendations**
  - **Varies depending on stackup**
  - **Typically rules of thumb say 3H spacing**
    - **For a 5 mil dielectric this would be 15 mils**
    - **For signals coupled closely to reference planes, often 1.5H can be used or ~8 mils**



Agenda

DDR Memory design



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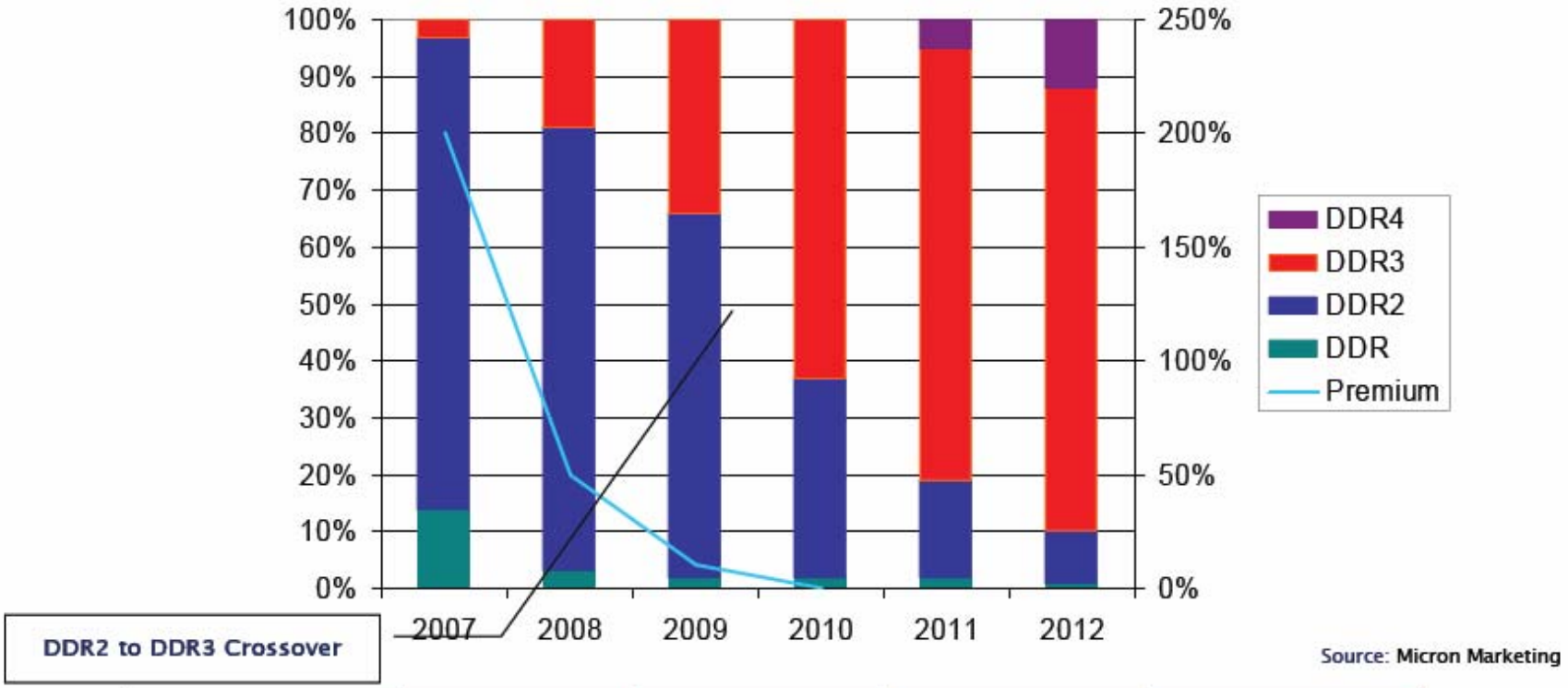
DDR Feature Comparison

	DDR	DDR2	DDR3
Data Rate	200 - 400 Mbps	400 – 800 Mbps	800 – 1600 Mbps
System support	4 slots – 8 loads	2 slots – 4 loads	2 slots – 4 loads 1600 Mbps = 1 slot
Signaling Technology	SSTL_2	SSTL_18	SSTL_15
DQS signals	Bi-directional single ended	Bi-directional single or differential	Bi-directional differential
ODT	No	Yes	Yes
Signal leveling	No	No	Yes

DDR Market Trends

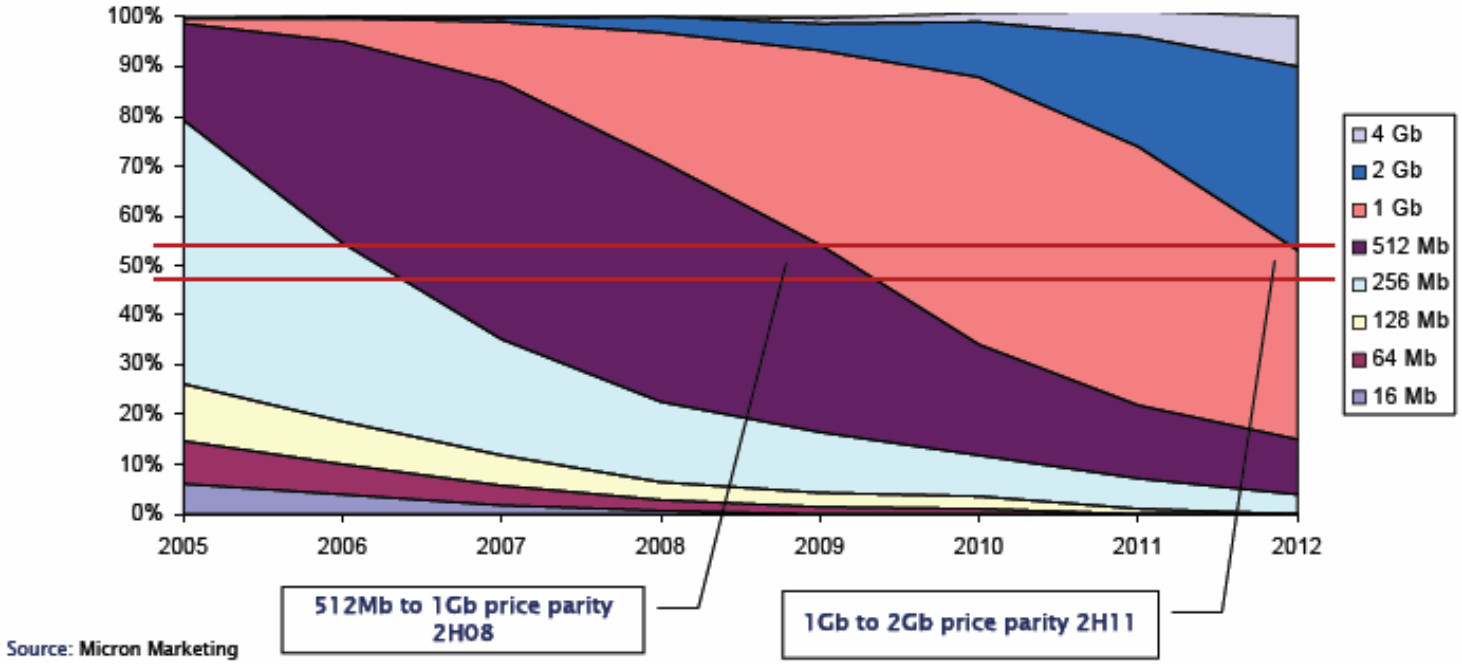


Source: Micron Marketing

	2007	2008	2009	2010
DDR	14%	3%	2%	1%
DDR2	83%	78%	64%	33%
DDR3	3%	19%	34%	60%

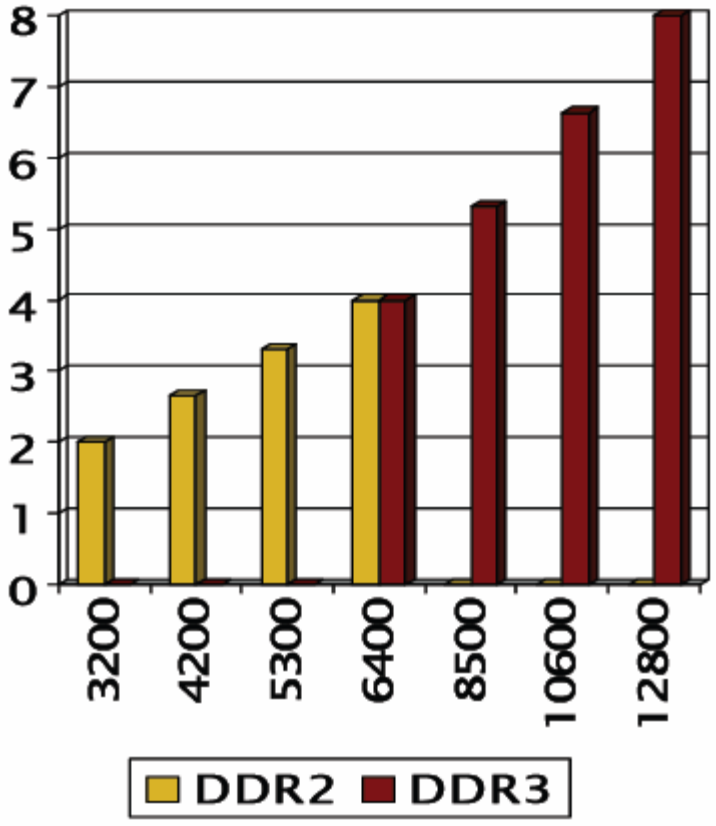
DDR3 Market Trends

- **Main growth in the 512 Mb and 1Gb memory modules**
  - **Early adopters starting with 256 Mb modules**



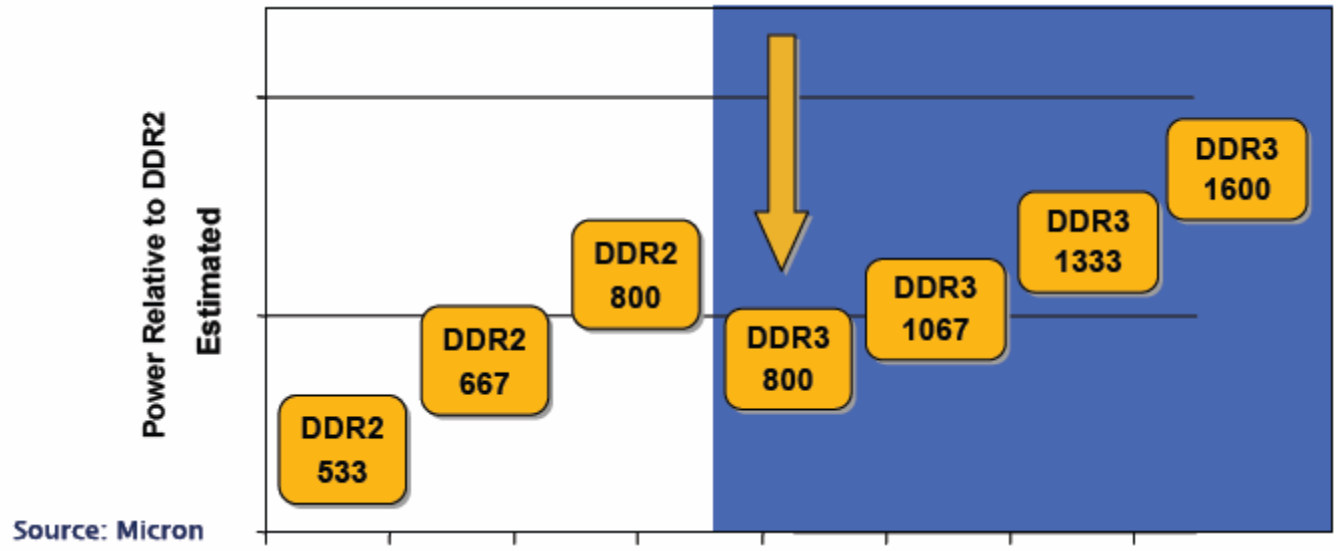
DDR3 Performance

- DDR3 has a peak transfer rate of 1600 MT/s
  - 800 MHz clocks
  - Provides a 2X bandwidth increase over DDR2
  - Maximum bus bandwidth of 12,800 MT/s
- 4 operating speeds for DDR3
  - 800 MT/s
  - 1067 MT/s
  - 1333 MT/s
  - 1600 MT/s



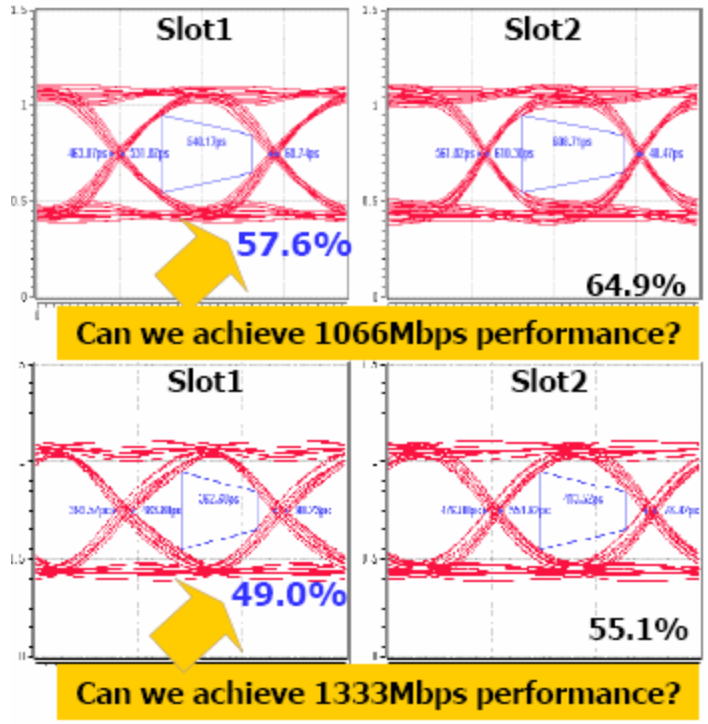
Lower Power

- **Supply voltage reduced from 1.8V to 1.5V**
  - **30% reduction in power supply voltage**
- **Higher impedance driver requires less current**
  - **Driver impedance of 34 ohms vs. 18 ohms in DDR2**



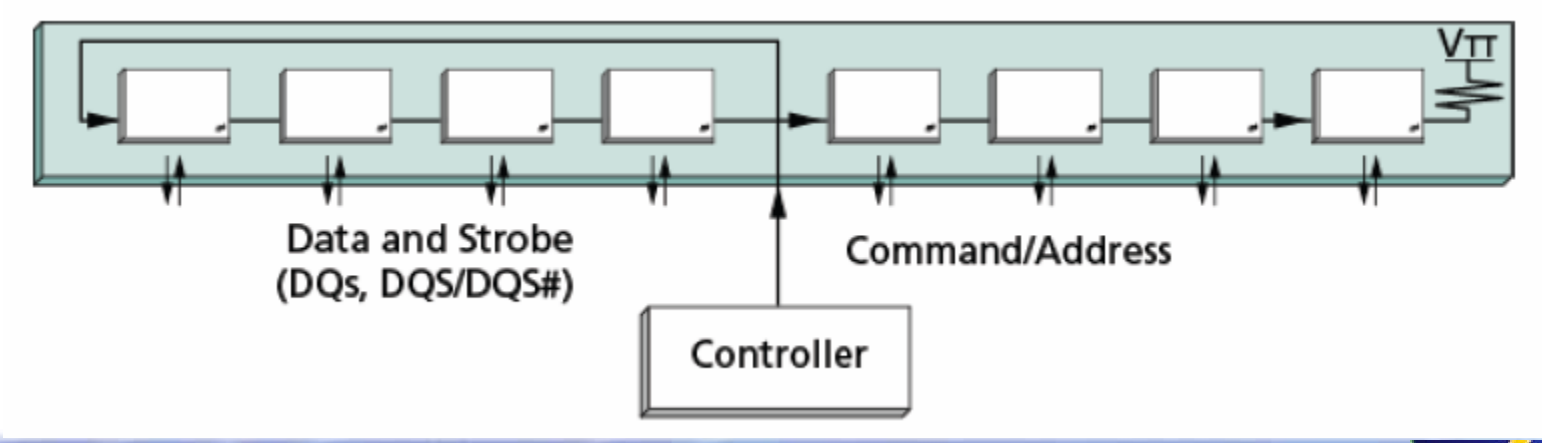
DDR3 Architecture

- 800 MT/s – 1333 MT/s will support 2 DIMM slots
  - Margins will be tight for 1333 MT/s on Read operations
- 1600 MT/s only supports 1 DIMM slot
  - Can not achieve reliable data transfer with 2 slots



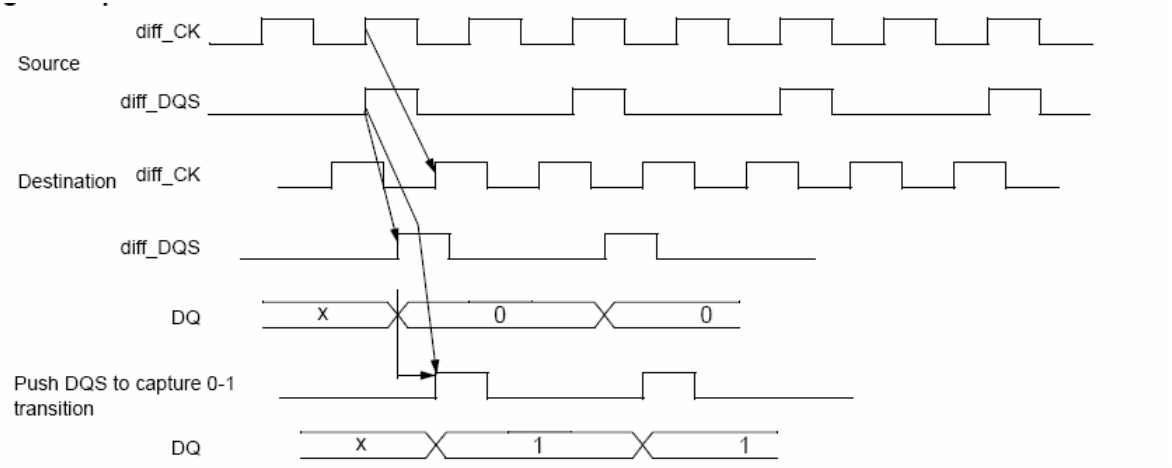
Fly-by Architecture

- **Address, Control, and Clocks use Fly-by architecture vs. branch architecture for routing**
  - **Daisy-chain topology for these signals**
- **Provides improved signal quality**
  - **Reduces number of stubs and their length**
- **Requires write leveling to optimize timing**
  - **Fly-by creates too much skew between clock and strobe**



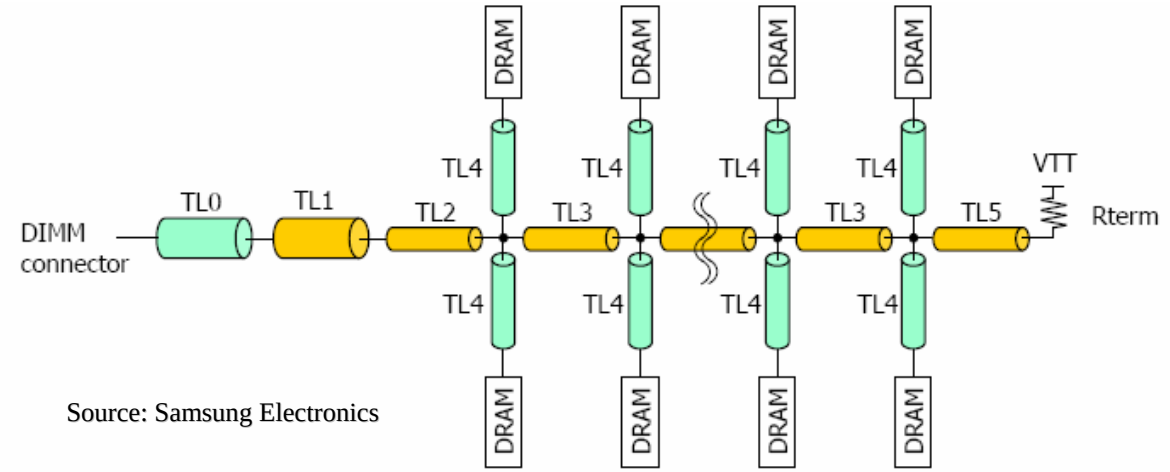
Write Leveling

- **Write leveling adjusts the DQS to CK relationship by the controller**
  - **Uses a simple feedback provided by the DRAM**
- **Memory controller has an adjustable delay setting on DQS**
  - **Used to align the rising edge of DQS with the clock at the DRAM pin**
- **DRAM asynchronously feeds back CK sampled with the rising edge of DQS**
- **The controller repeatedly delays DQS until a transition from 0 to 1 is detected and determines DQS delay**



Termination

- **On-Die Termination used for Data/Strobes**
  - **Dynamic and controllable as in DDR2**
- **Address, Command, and Control signals no longer require pull-up terminations on PCB**
  - **Termination is on DIMM module**
    - **39 ohm pull-up termination**

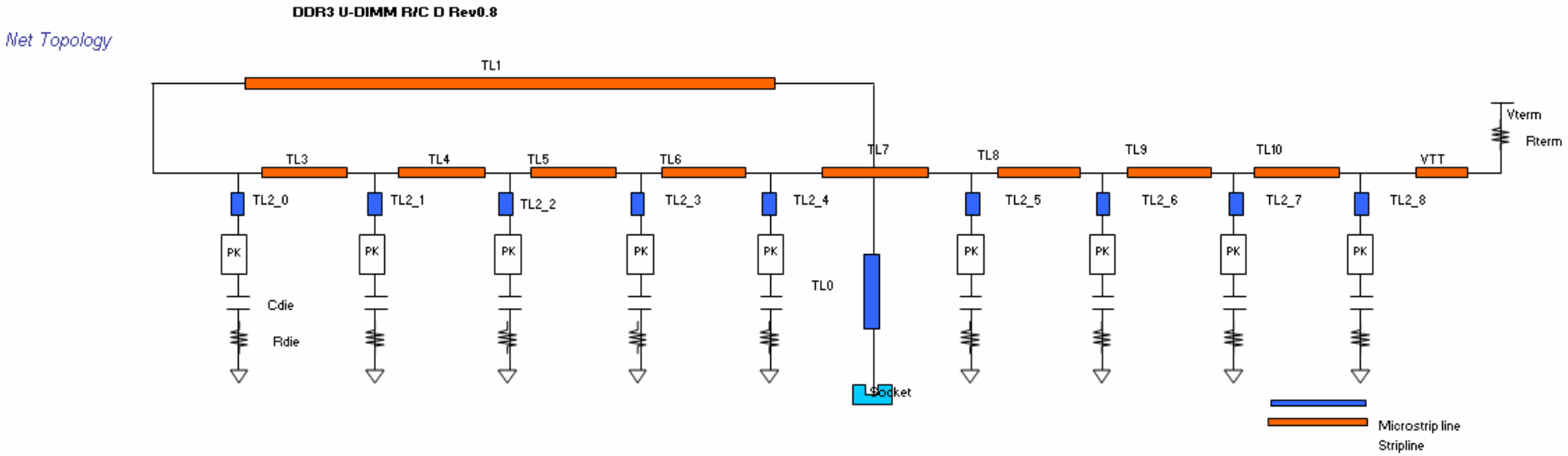


Source: Samsung Electronics

Lead-in vs. Loaded routing

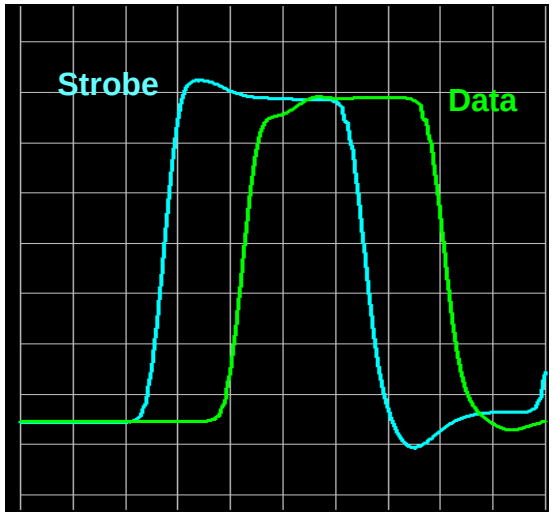
- **Neck down traces on DIMM modules to compensate for capacitive loads**
  - **Increases impedance on traces**
  - **55 ohms on PCB and 60 ohms on module**

$$Zo = \sqrt{\frac{L}{C}}$$



Agenda

DDR Memory design



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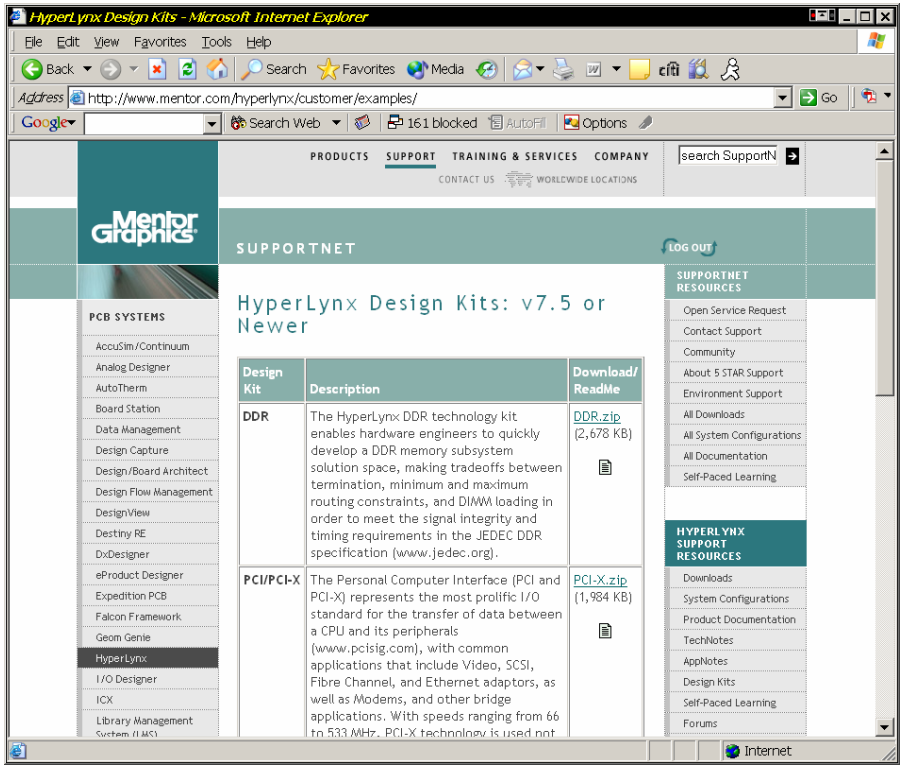
Summary

- **DDR and DDR2 designs**
  - **Data/Strobe signals tend to be easier to route for SI**
    - **Want to minimize skew in the byte lanes**
  - **Address/Control signals have most SI problems**
    - **Due to loading conditions and branch topologies**
      - **Signal always worst at the first DIMM module**
- **DDR3**
  - **No real layout guidelines available yet since the technology is still being developed**
    - **Expect heavy adoption in 2009**

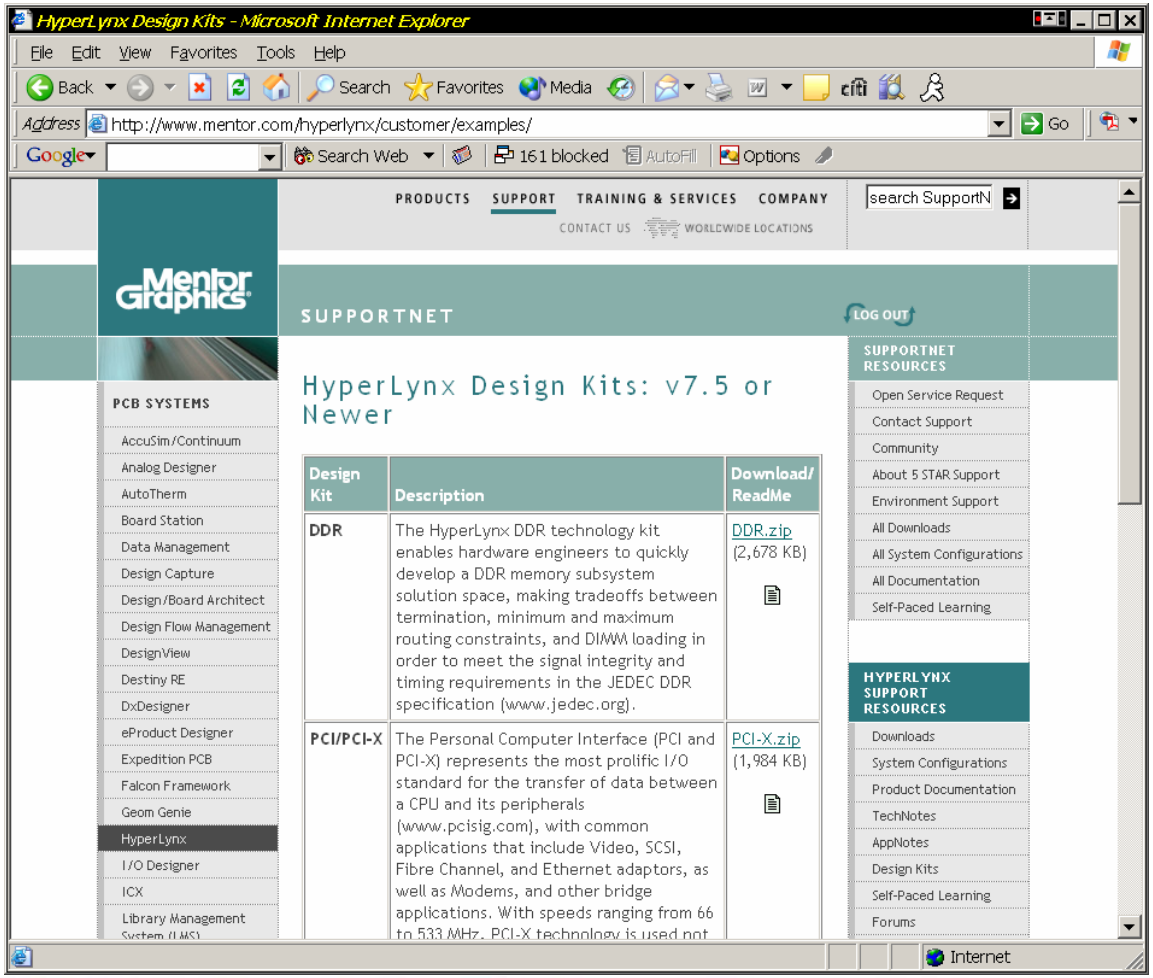
Additional Technology Design kits

- USB
- DDR
- DDR2
- PCI/PCI-X
- SATA
- PCI Express
- FibreChannel
- SAS
- Embedded DDR
- HyperTransport
- HDMI



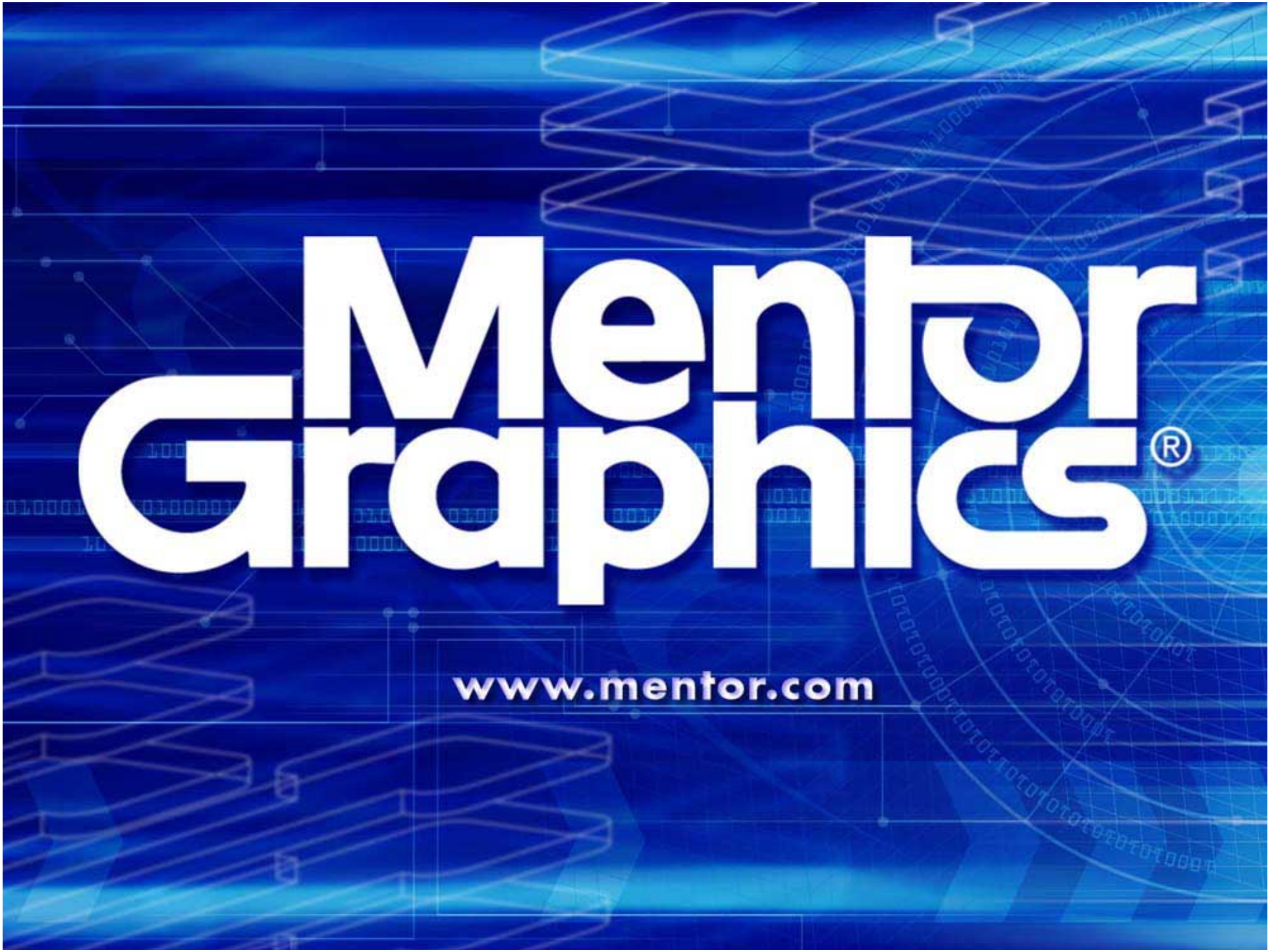
HyperLynx Design Kits

http://www.mentor.com/hyperlynx/customer/examples/



Acknowledgments

- **Special thanks to Micron for providing a majority of the DDR3 content and DDR2 routing guidelines**
  - **Reference their DDR3 Advantages presentation**
  - **www.micron.com**
- **Samsung Electronics**
  - **Providing feature comparison and topology and impedance information for DDR3**
  - **www.samsung.com**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